CLOCK Designer™

VLSI Clock Design-Planning Tool

OEA International, Inc.

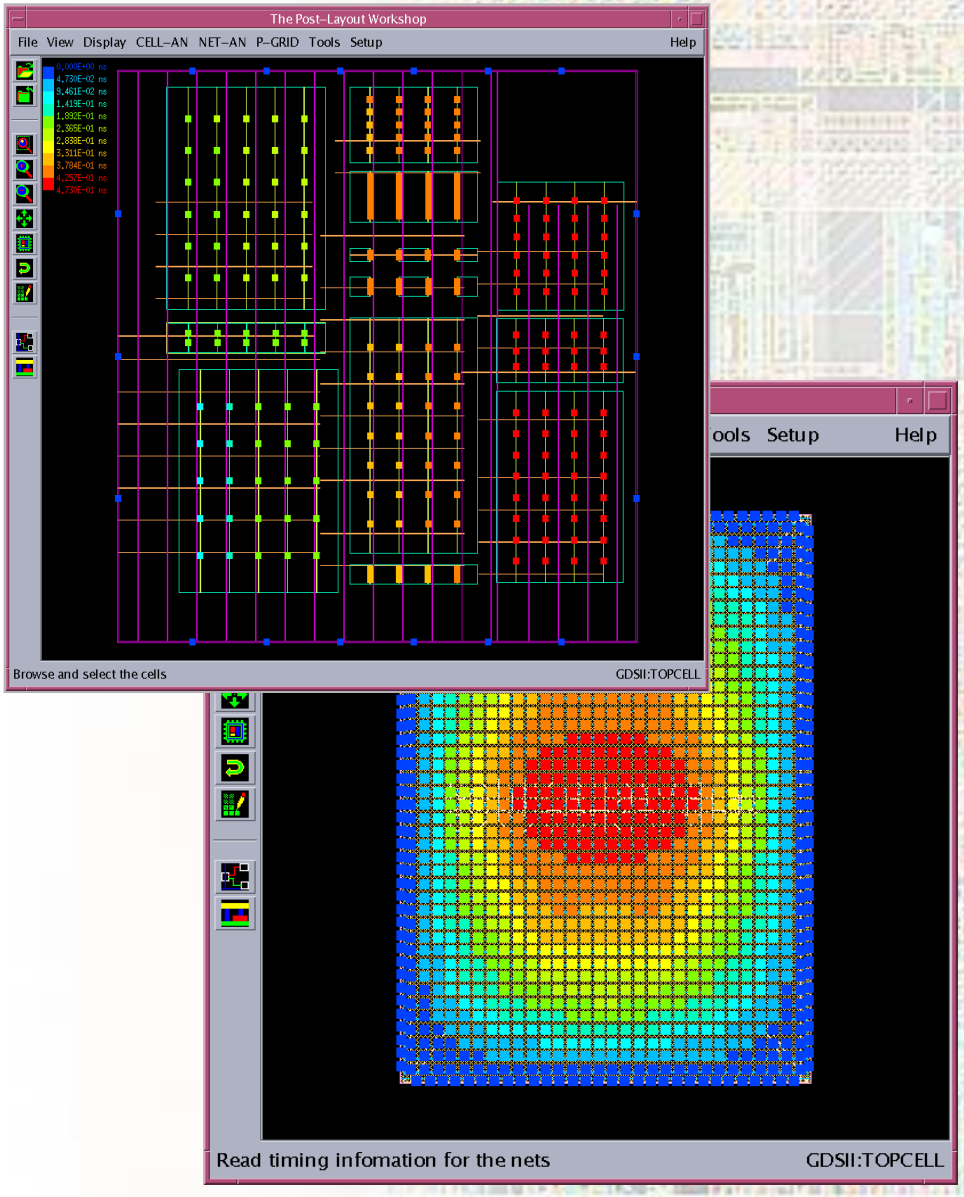
155 East Main Ave, Suite 110

Morgan Hill, CA 95037

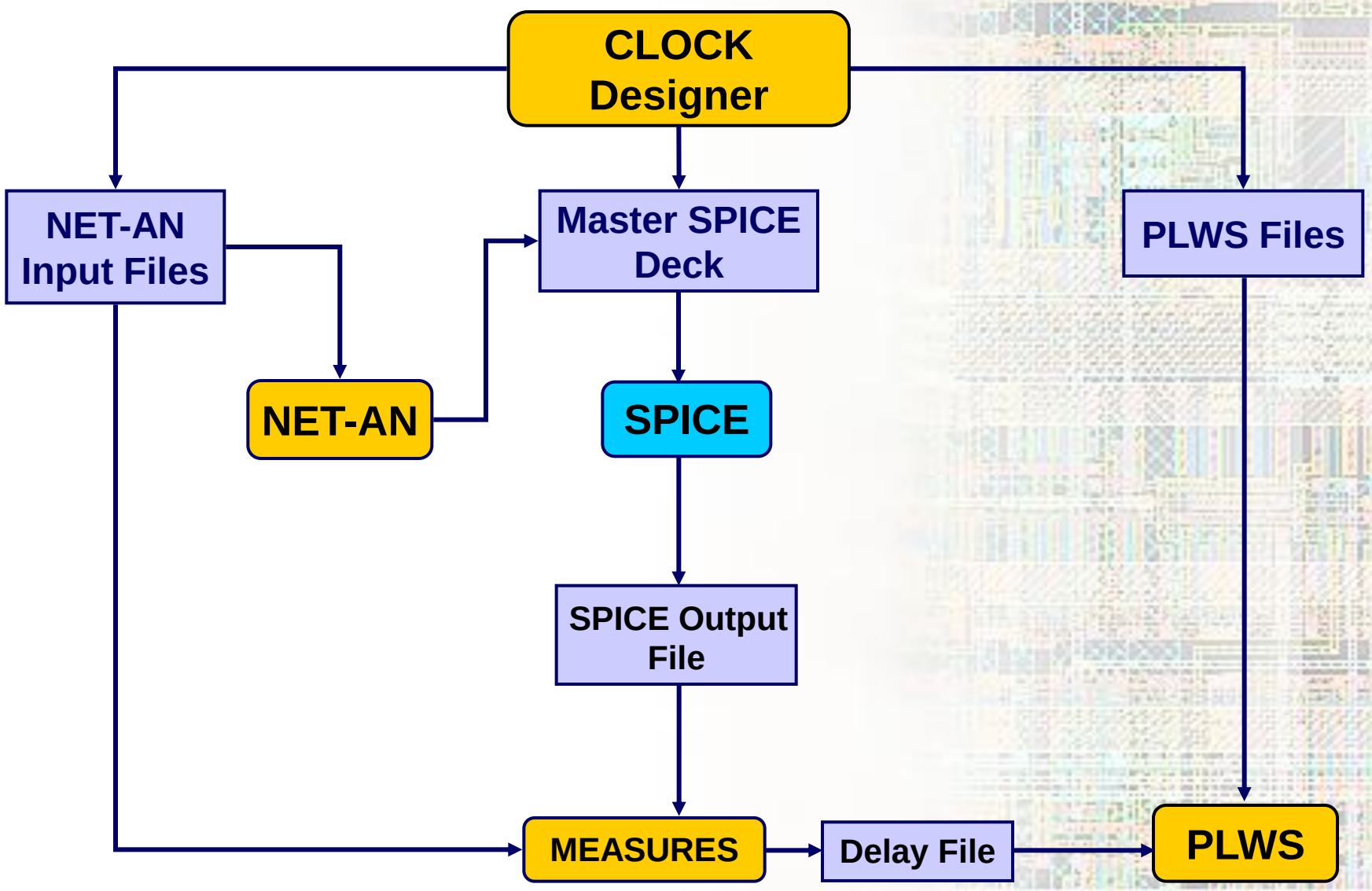
www.oea.com

CLOCK Designer Features

- Complete fast full circle creation of planned clock layout, accurate extraction, circuit analysis, and color coded visual feedback
- Supports design of Gridded and Spine type clock routing strategies
- Works with OEA NET-AN to extract accurate 3D RCLM parasitic network and SPICE to simulate precise predictions of delay and skew
- Fast cycle time for quick what-if analysis to optimize clock network widths, spacing, and buffer locations
- Fast trade-off analysis of driver strength versus skew and/or power
- Runs on all popular workstation platforms

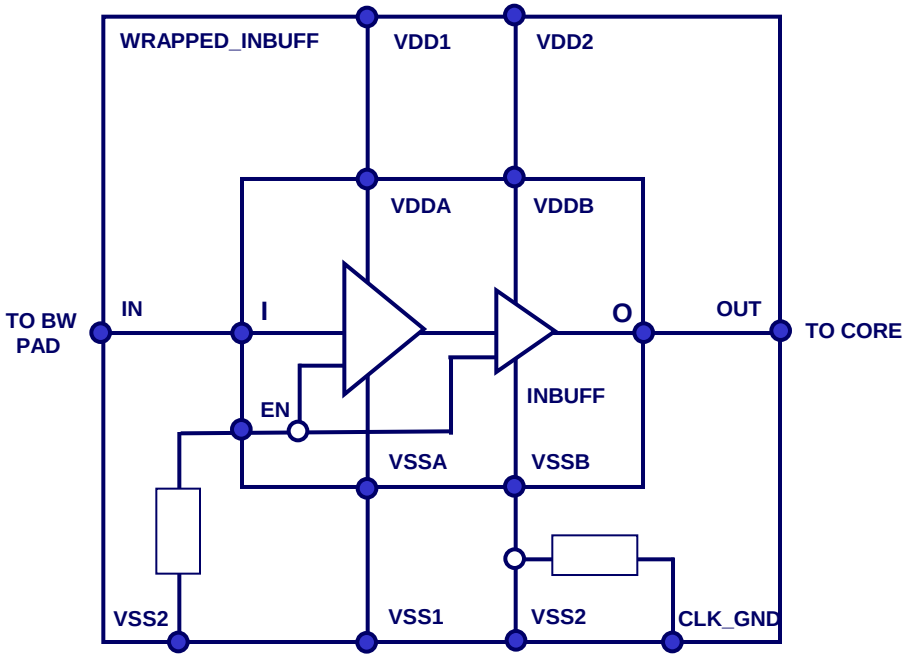


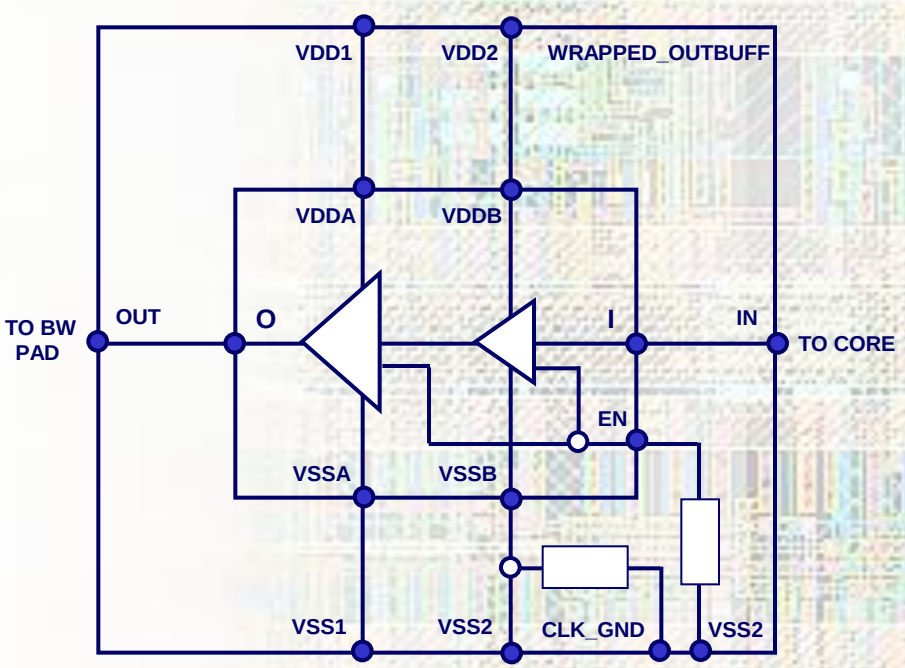
Usage Flow to Obtain Skew/Delay from NET-AN



Example of Wrapper Circuits

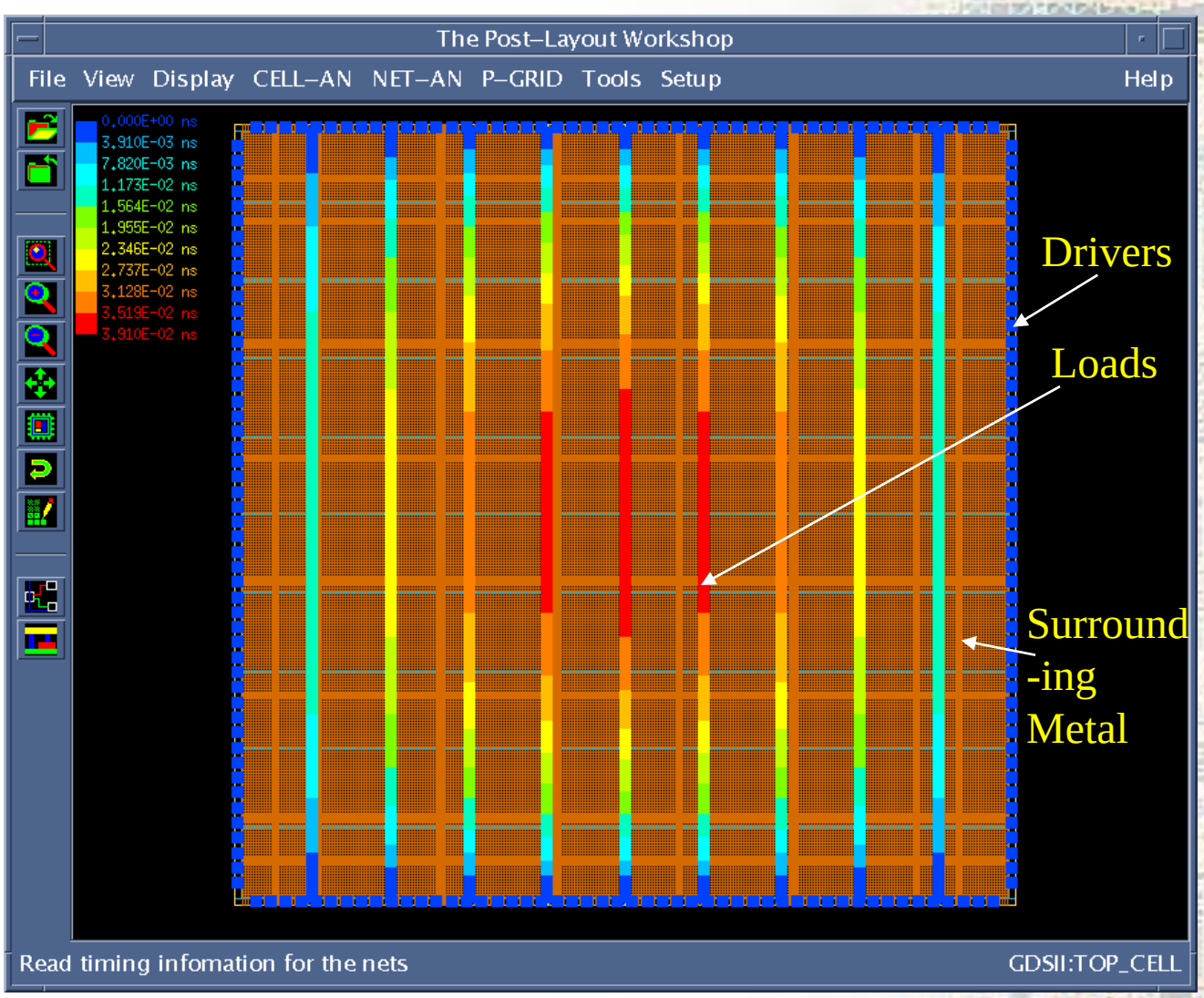
Used to Tie Off Unused Pins, Match Ring Names with Voltages, Keywords for 'IN', 'OUT' and 'CLK_GND' Pins



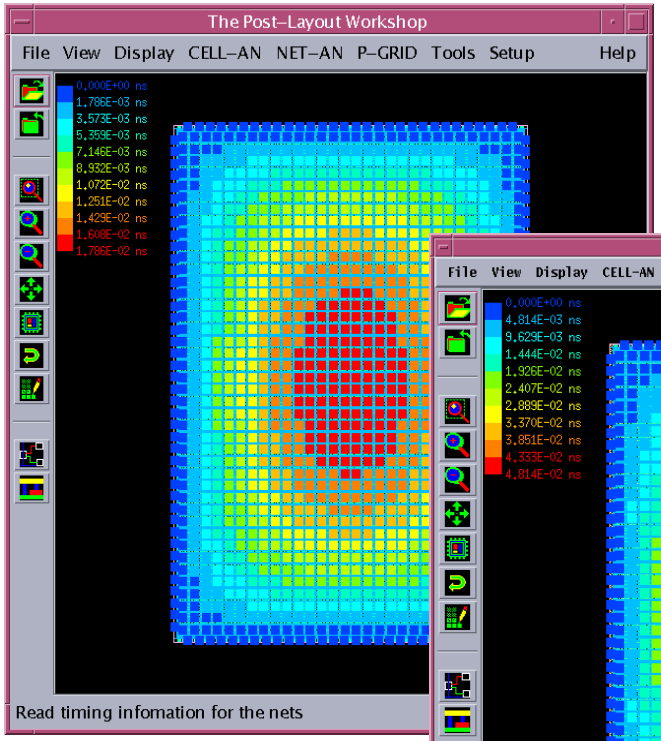



```
•  SUBCKT     WRAPPED_INBUFF  IN   OUT   VSS2   VDD2   VSS2   VDD1   VSS1   CLK_GND
R1      VSS2      CLK_GND      0.001
R2      VSS2      EN                    0.001
X1      IN      OUT      VSS2      VSS2      VDD2   VSS2   VDD1   VSS1   INBUFF
ENDS
SUBCKT INBUFF      I      O      EN      VSSB      VDDB      VSSA      VDDA
…
…
ENDS
```

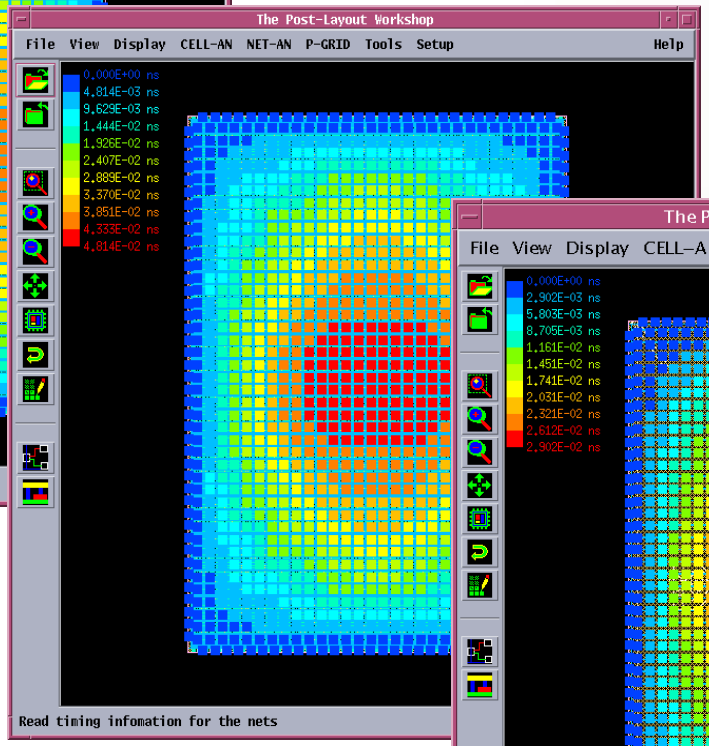
Example of Full Chip Clock Planning Delay Results



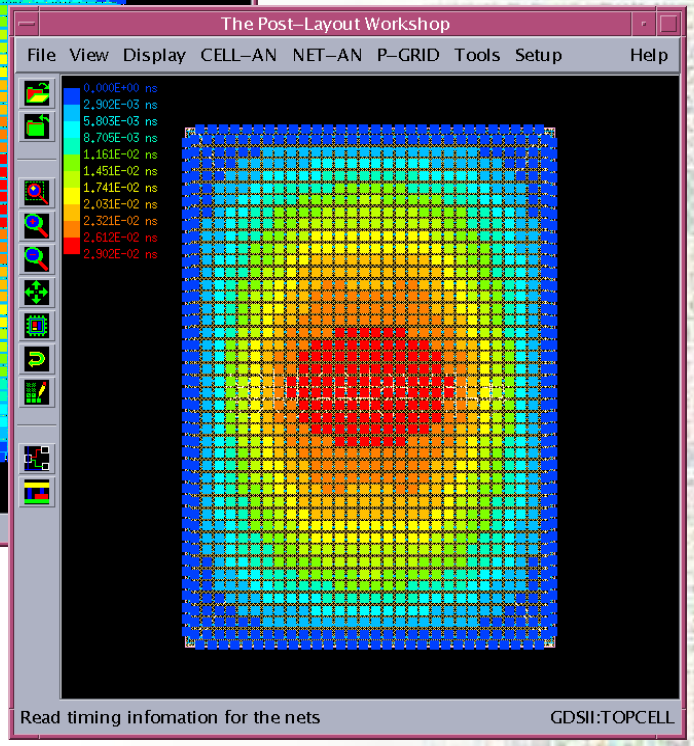
Example of Importance of Inductance using CLOCK Designer



RC skew
17.86 ps



RCL skew
48.14 ps



RCLM skew
29.02 ps