FABLESS SEMICONDUCTOR ASSOCIATION

SPIRAL and RF-PASS Three Dimensional Design and Analysis Tools for RF Integrated Circuits

By

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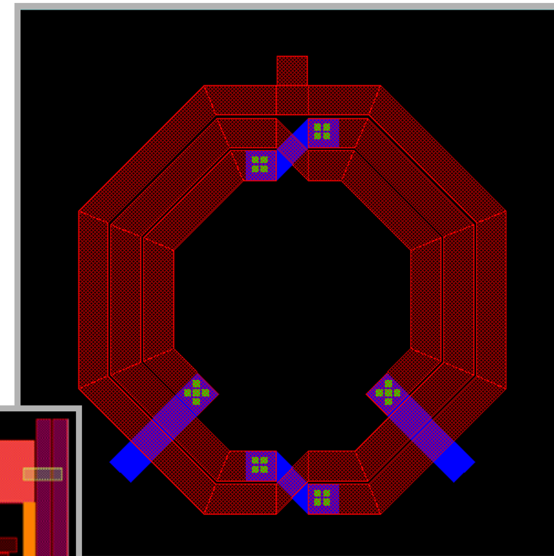
Agenda

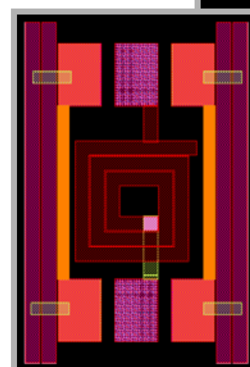
- Introduction to On-chip RF Components
- On-chip Inductors
- Why can not we use Pre-characterized Inductors
- Inductance Concepts
- Test Chip Results
- A Real Spiral Inductor Design
- Simplified “curve-fit” Model Generation
- On-chip Capacitor Designs
- Conclusions

OEA RF/Analog Software Products



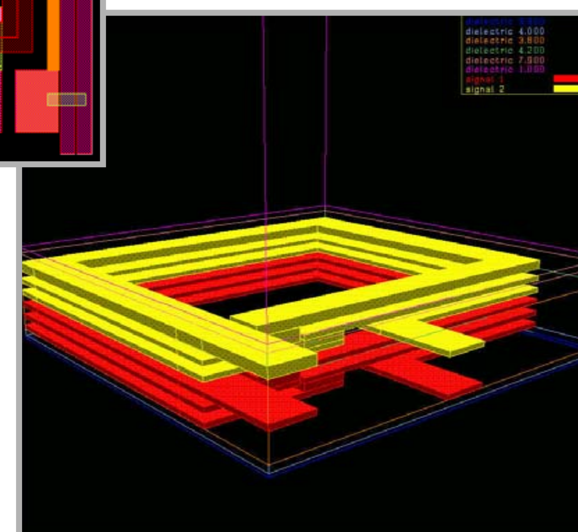
SPIRAL™

- Includes all relevant effects (skin, substrate, etc…)
- Synthesizes a large variety of inductors
- Can examine thousands of designs in a few hours
- Generates layout, Spice, Z & S parameters
- Can fit to many simplified models
- Optimization engine included



RF-PASS™

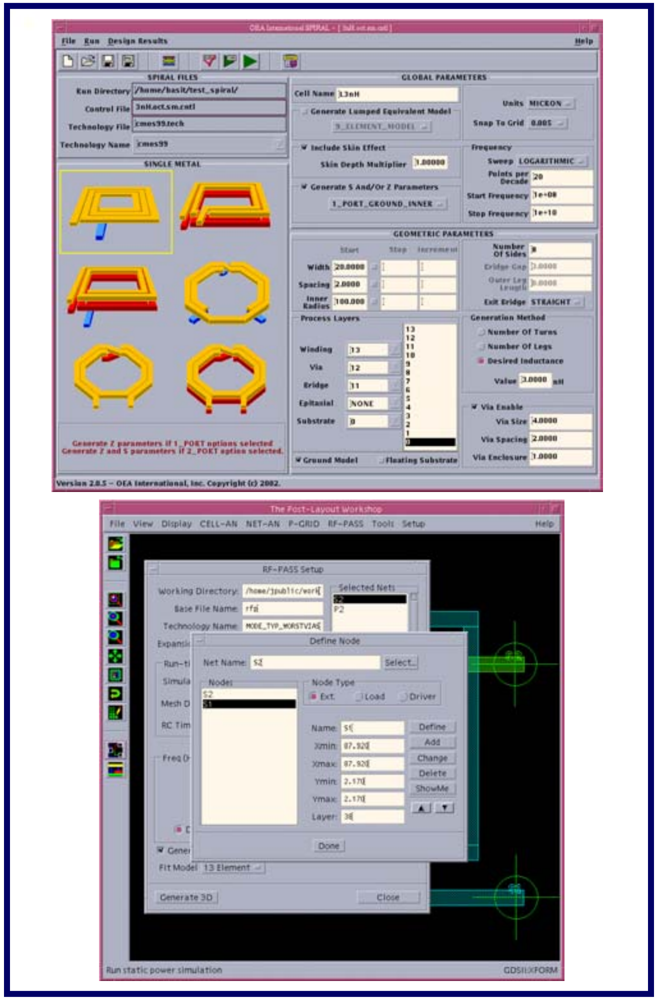
- Outputs N-Port Y, Z and S parameters
- Handles much more complex substrates and designs
- Optimization of arbitrarily complex passive structures



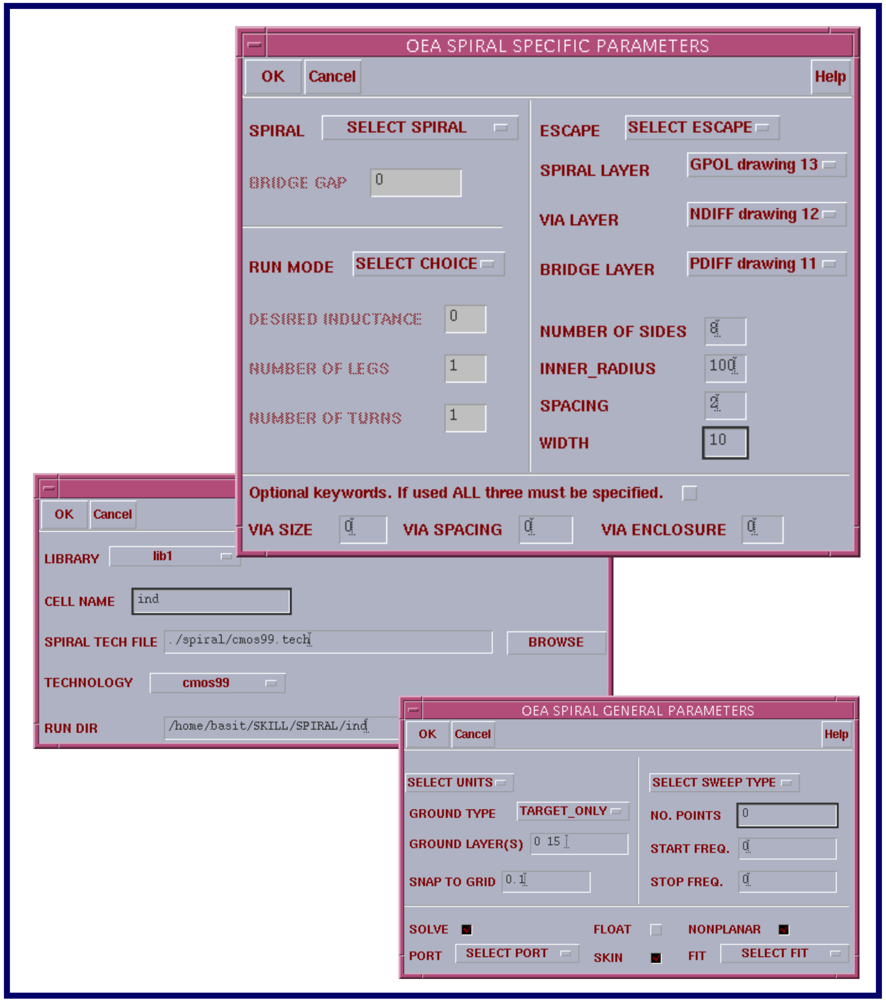
SUBSTRATE NOISE ANALYSIS

- Calculates full-chip substrate noise couplings
- Enables what-if exploration of isolation strategies
- Allows design planning before layout

OEA RF/Analog Software Products

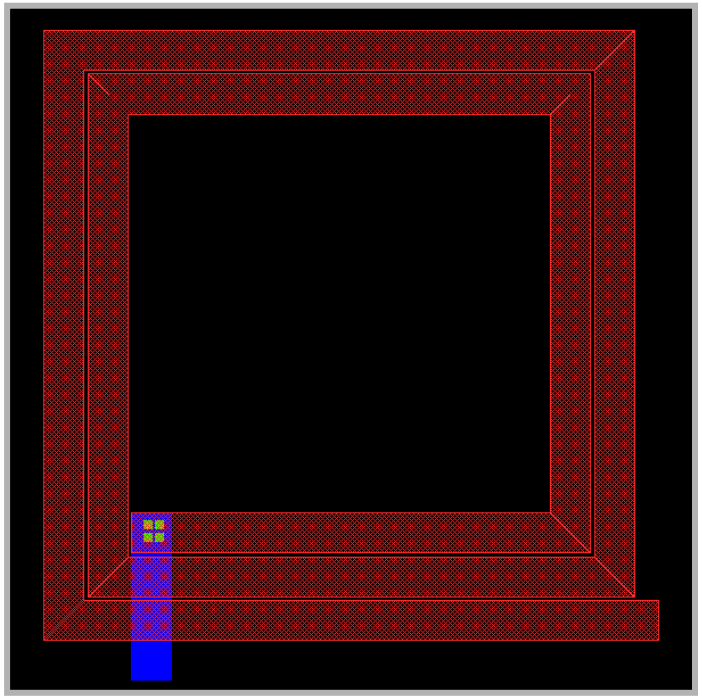


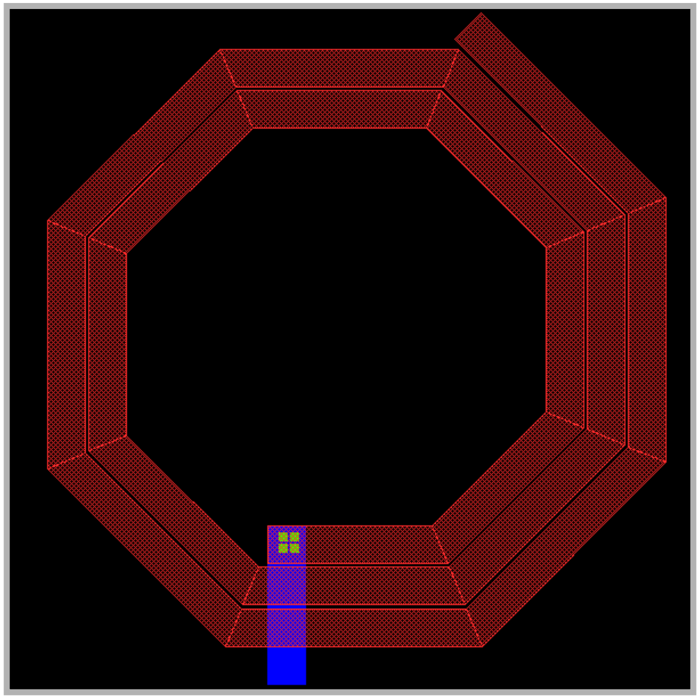
Generic UNIX Interfaces



Cadence Interface

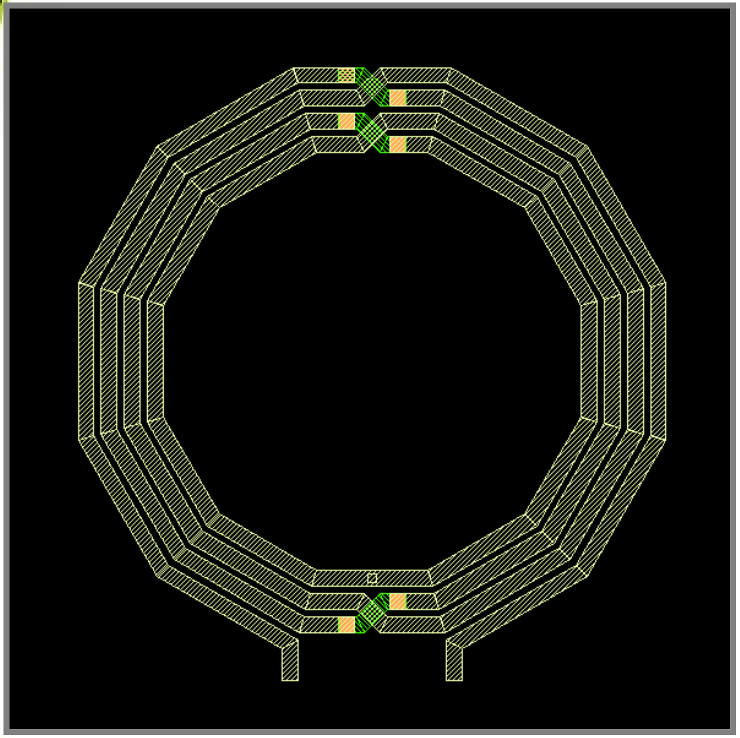
Standard Inductors: 4 sided / 8 sided

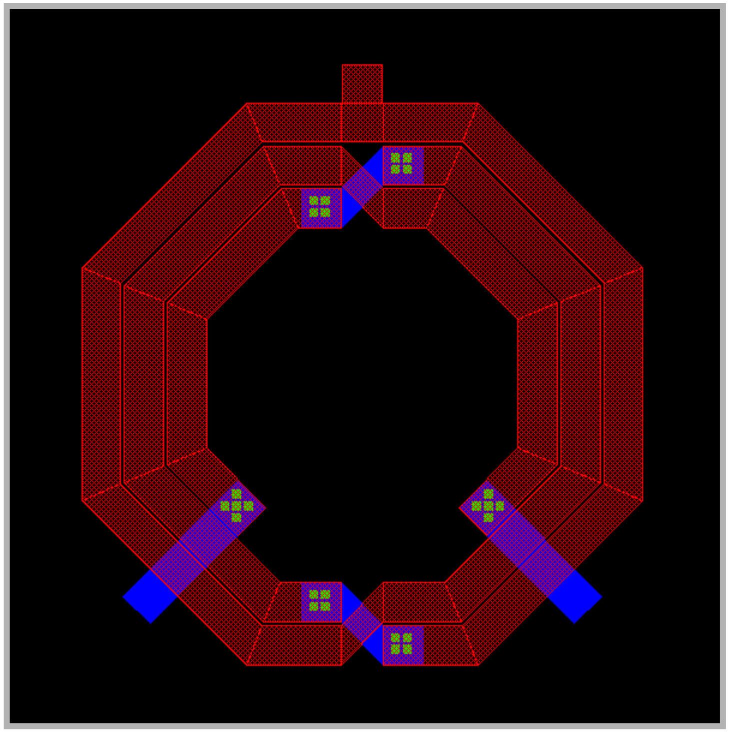




- **Usually uses top metal layer for winding**
- **Can use multiple metal layers in parallel**
  - Lowers series resistance
  - Increases capacitance
- **Can use multiple metal layers in series (coil)**

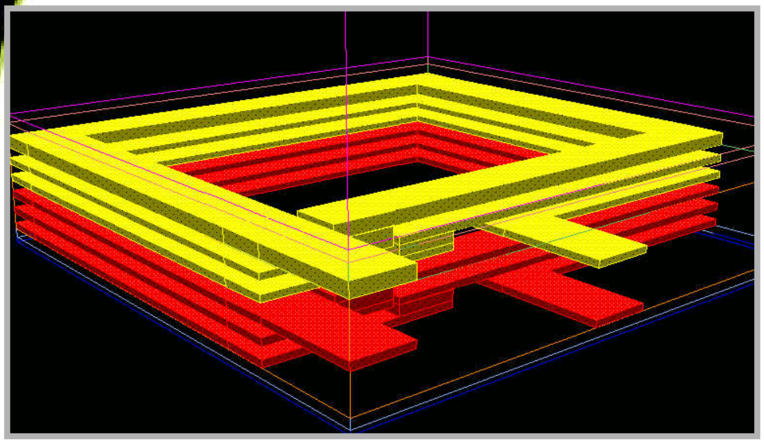
Symmetric Differential Inductors

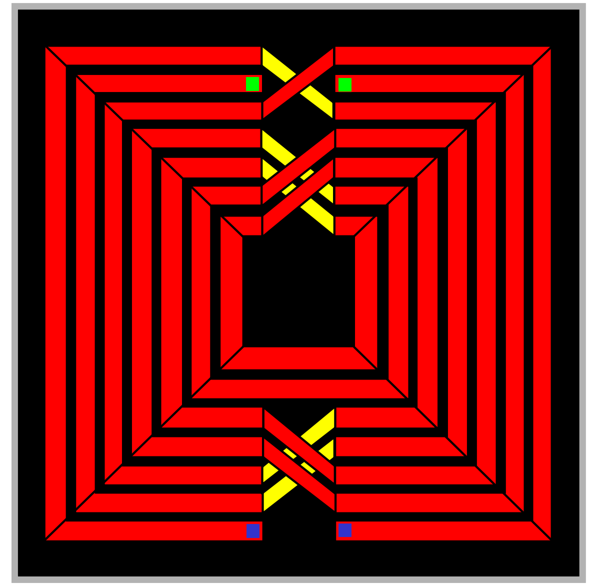


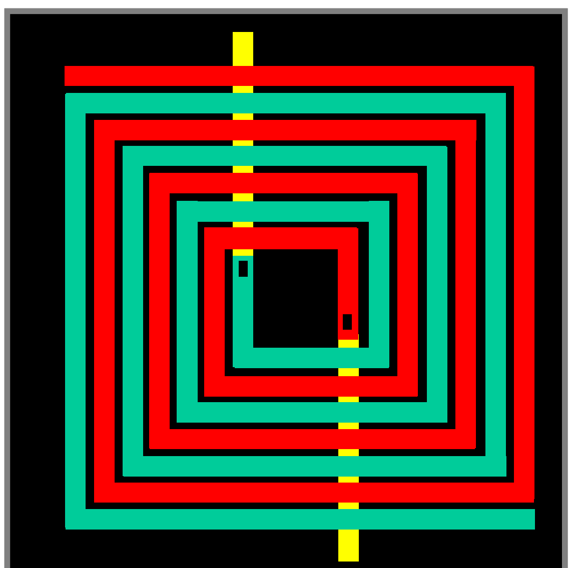


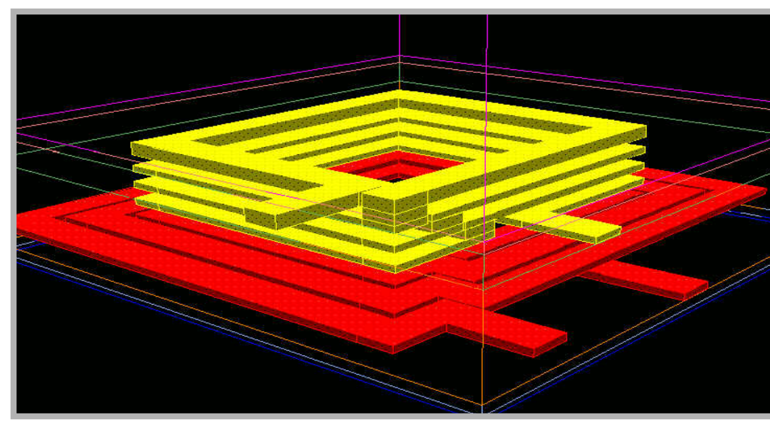
- **Symmetric Center Tapped Inductors instead of 2 'uncoupled' inductors:**
  - Easily defined center tap
  - Reduced chip area
  - Higher Q (reduced substrate losses)
  - No need to model parasitic coupling

Transformers and Baluns

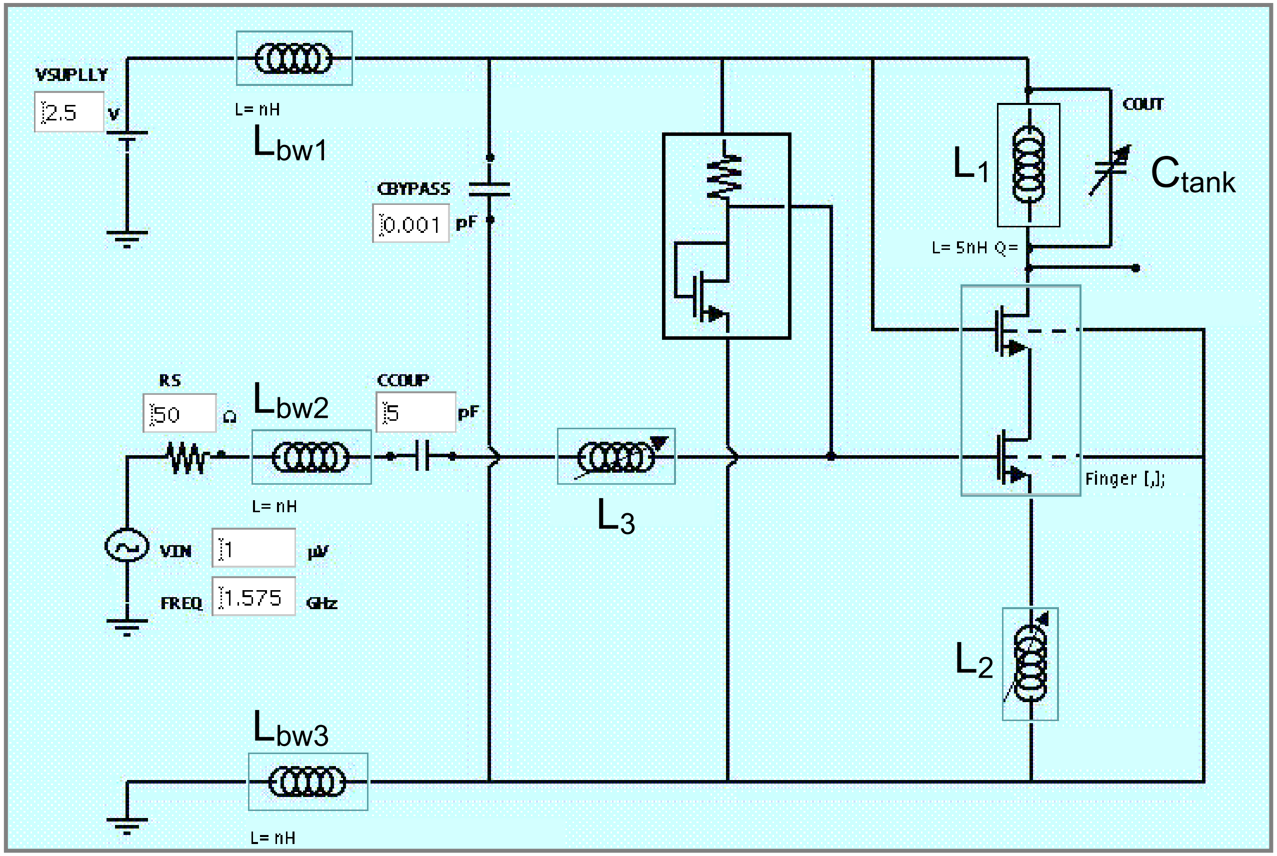






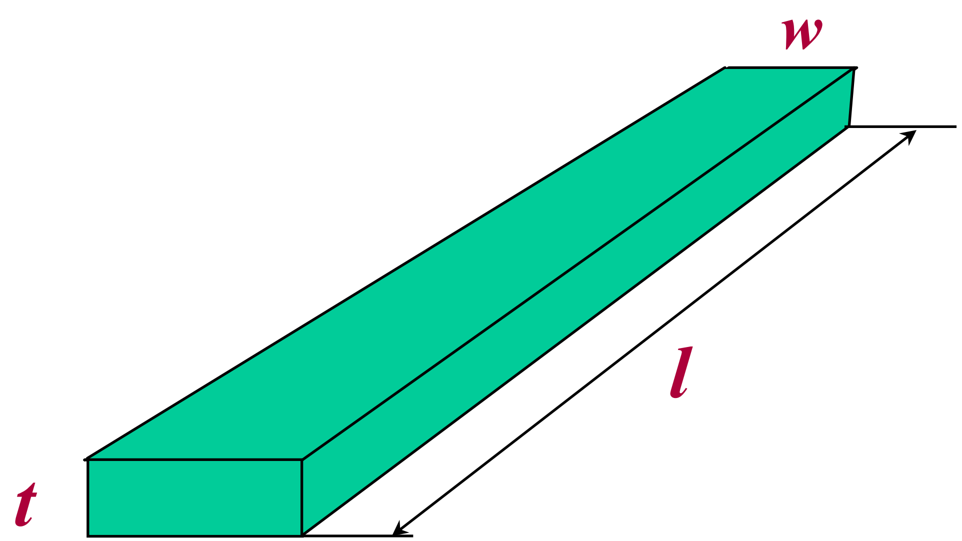


CMOS LNA Example to Show one can not use Pre-characterized Inductors for an Optimal Design !



L_1, L_2, L_3, C_{tank} and Transistor Sizes are all related!

Inductance of a Rectangular Conductor



$$L(\mu H) = 0.002l \left\{ \ln\left[\frac{2l}{(w+t)}\right] + 0.5 - k \right\}$$

Where $k = f(w,t)$

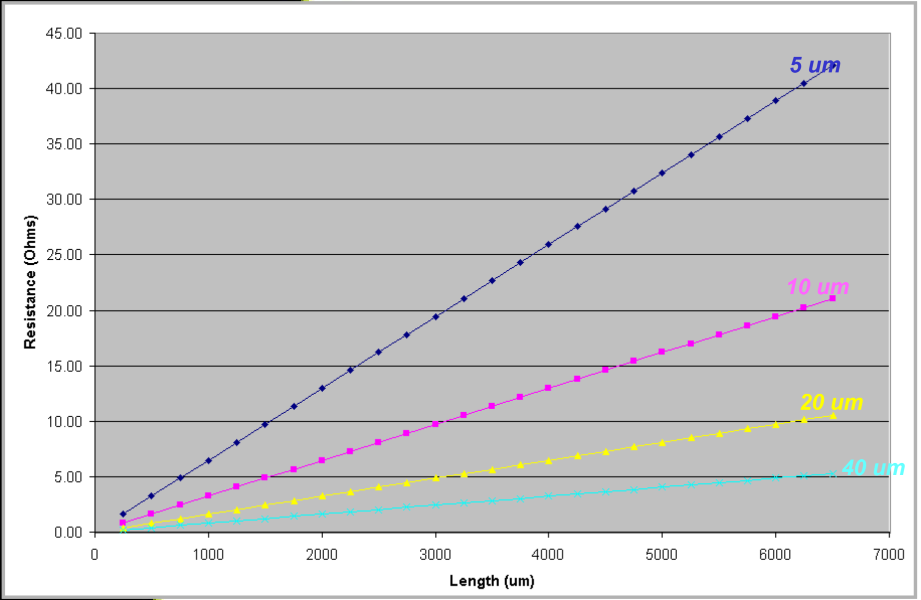
$0 < k < 0.0025$

l,t,w in cm

$$R(\Omega) = \frac{\delta l}{(w\,t)}$$

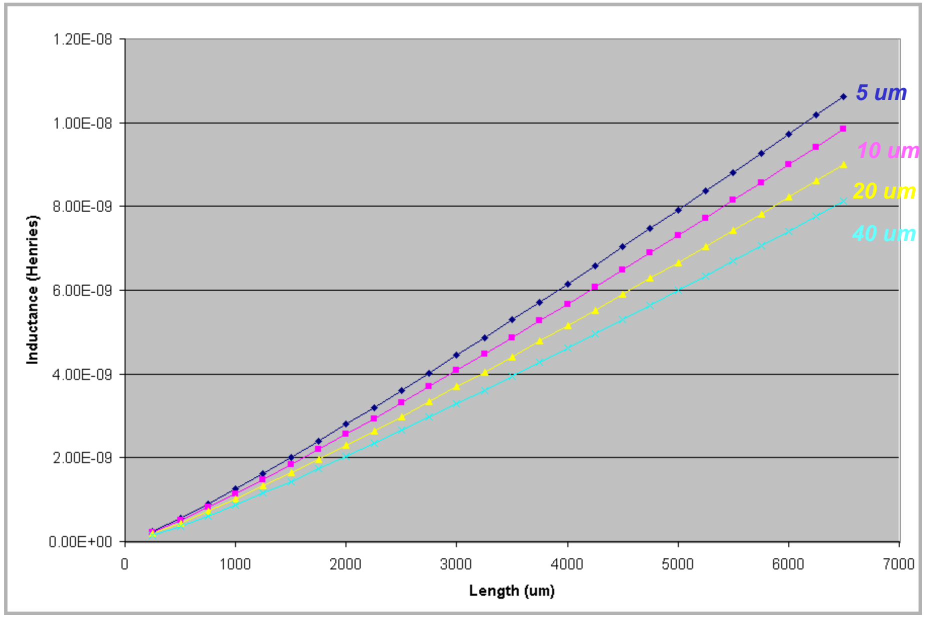
$$Z(j\omega) = R + j\omega L$$

Where $\omega = 2\pi f$



DC Resistance vs. Length at Various Widths (1 μm Thick Aluminum)

Inductance vs. Length at Various Widths



Q and *fpass* of a Rectangular Conductors

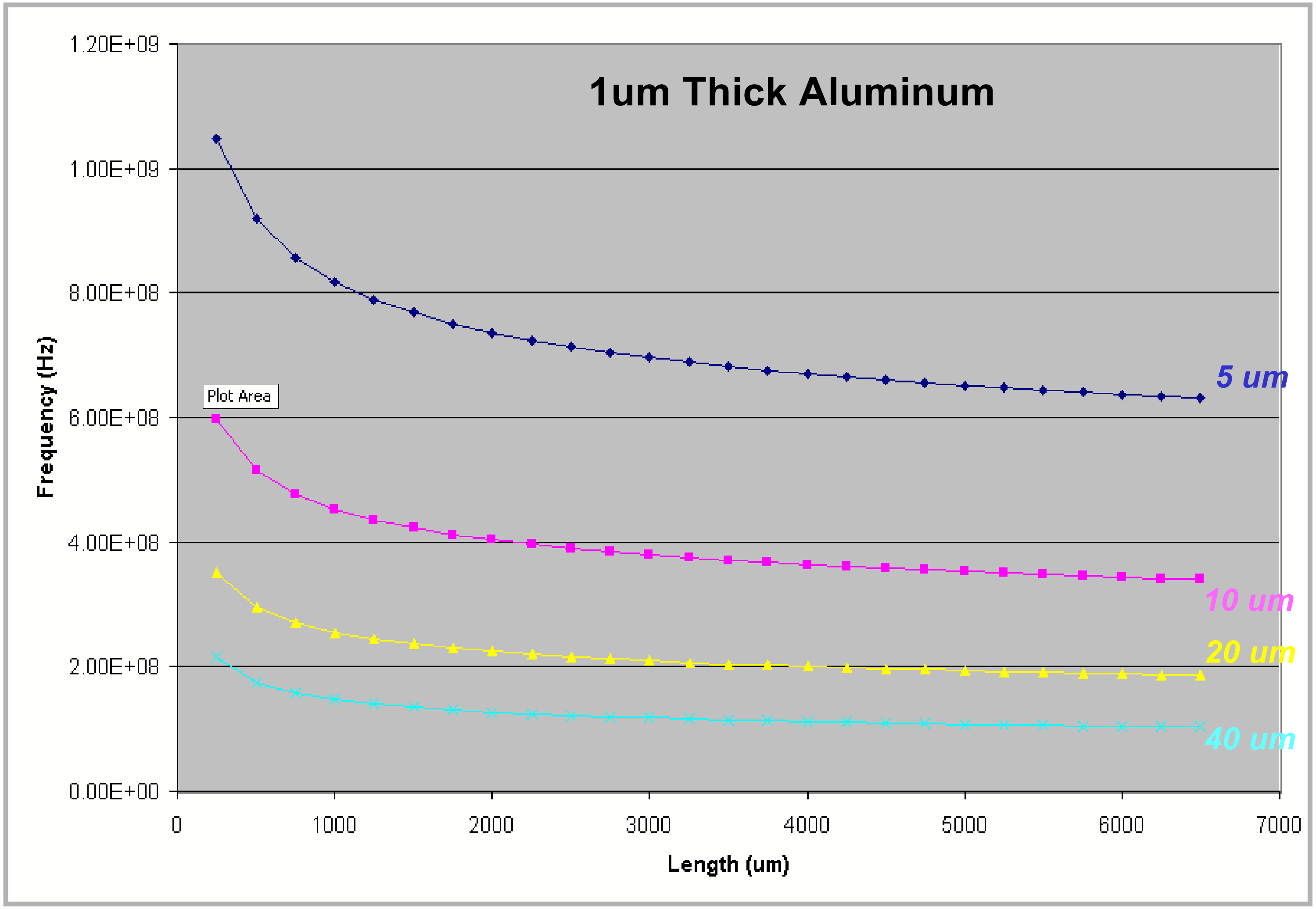
$$Q = \frac{I_m[Z(j\omega)]}{Re[Z(j\omega)]} = \frac{L\omega}{R} = \frac{L2\pi f}{R}$$

$$Q = \frac{0.002wt\,[\,ln\,(\frac{2l}{w+t}) + 0.5 - k\,]\,\omega}{\delta}$$

$$Q = 1 \Rightarrow f = \frac{R}{2\pi L}$$

$$f_{pass} = \frac{R}{2\pi L} = \frac{\delta}{0.002wt\,[\,ln\,(\frac{2l}{w+t}) + 0.5 - k\,]\,2\pi}$$

Minimum Frequencies for Onset of Inductive Behavior



Partial Inductance Approach

Six Self Inductances: $L_1, L_2, L_3, L_4, L_5, L_6$

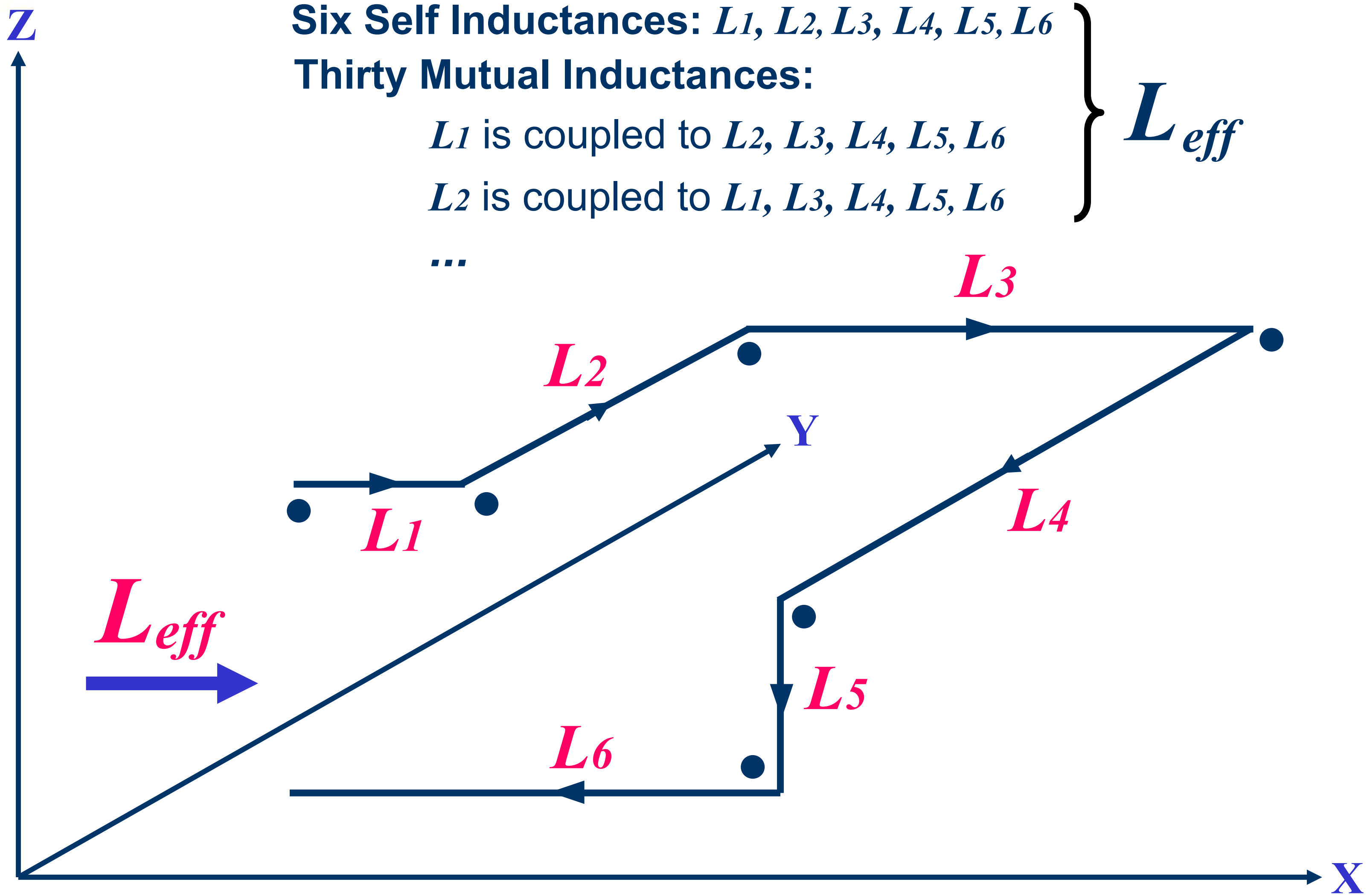
Thirty Mutual Inductances:

L_1 is coupled to L_2, L_3, L_4, L_5, L_6

L_2 is coupled to L_1, L_3, L_4, L_5, L_6

...

} L_{eff}



Inductance Matrix Representation

$$\begin{bmatrix} L11 & L12 & \cdots\cdots\cdots & L16 \\ L21 & L22 & \cdots\cdots\cdots & L26 \\ \vdots & & & \\ L61 & L62 & \cdots\cdots\cdots & L66 \end{bmatrix}$$

$$L_{eff} = \sum_{i=1}^{n} \sum_{j=1}^{n} L_{i,j}$$

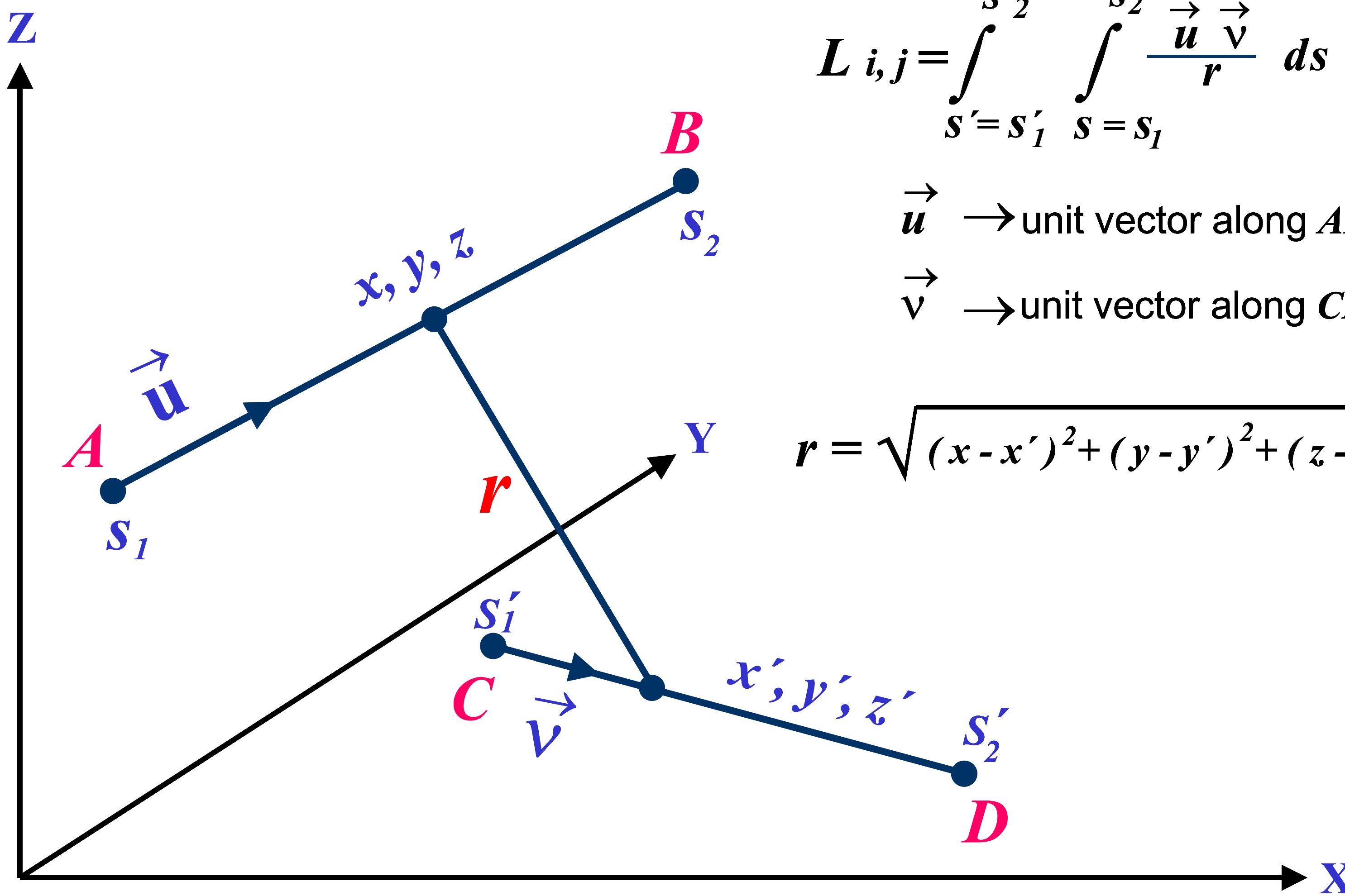
$$L_{i,j} = L_{j,i}$$

Self Inductance
Diagonals > 0

Off Diagonals
Mutual Inductance

Can have < 0, > 0, or 0 value in Henry

Neumann Formulation of Mutual Inductance



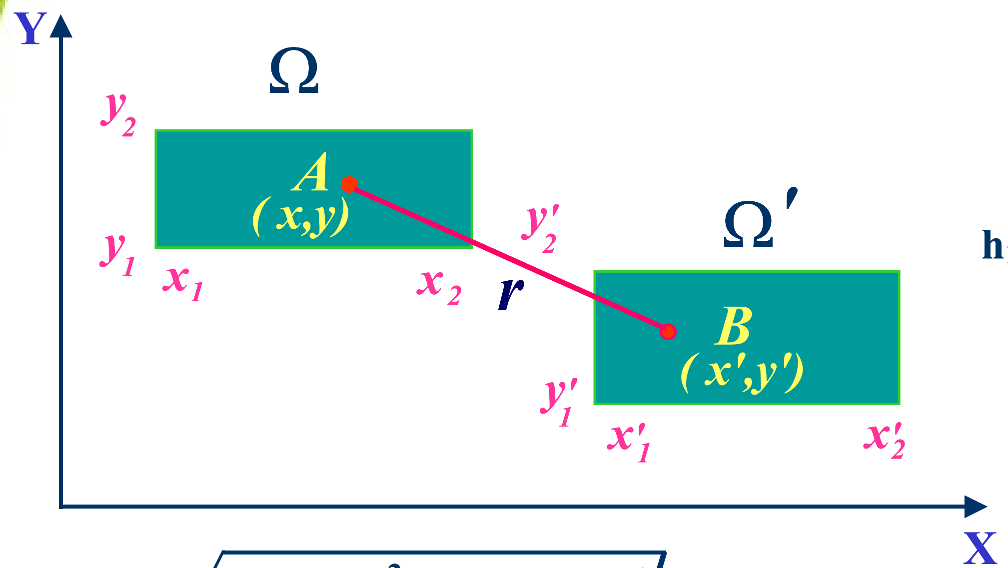
$$L_{i,j} = \int_{s'=s'_1}^{s'_2} \int_{s=s_1}^{s_2} \frac{\vec{u}\,\vec{v}}{r}\, ds\ ds'$$

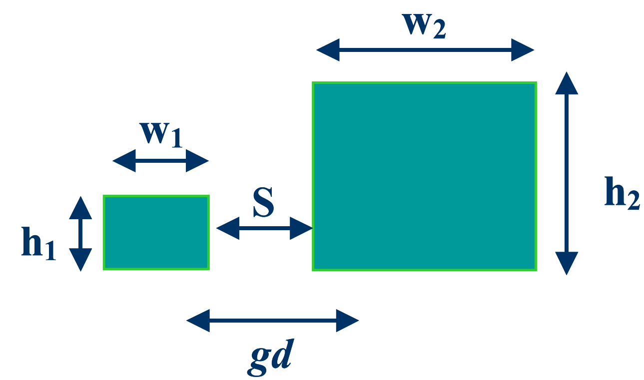
$\vec{u}$ → unit vector along AB

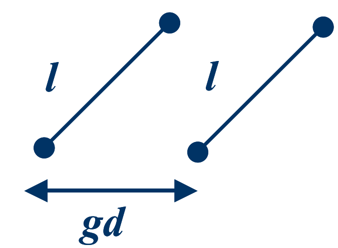
$\vec{v}$ → unit vector along CD

$$r = \sqrt{(x-x')^2 + (y-y')^2 + (z-z')^2}$$

Geometric Distance Between Objects





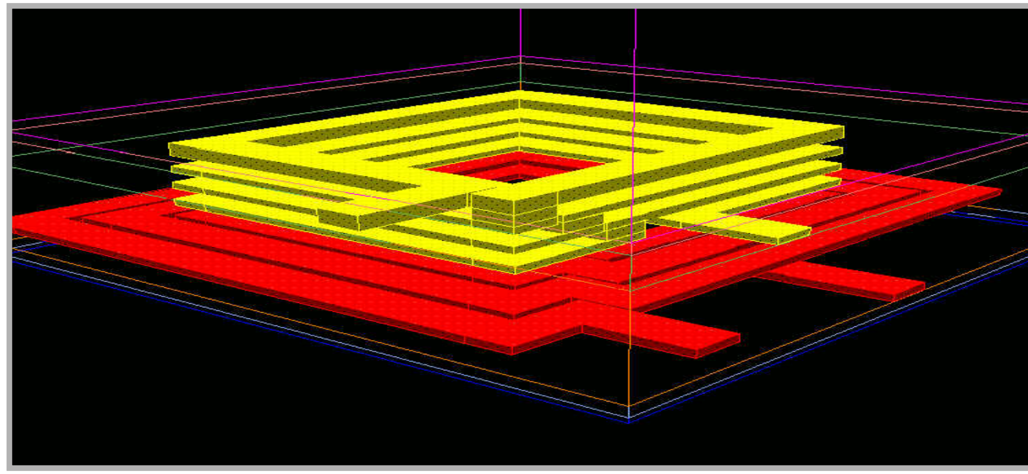


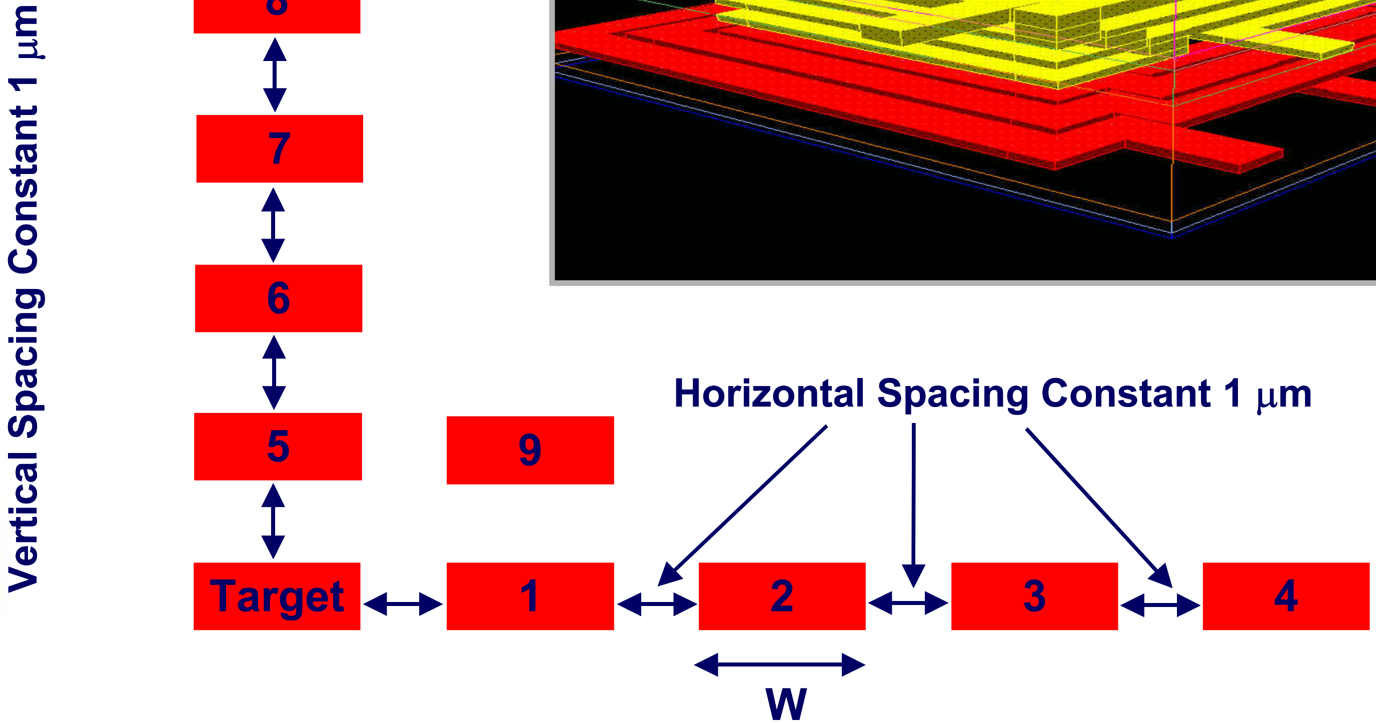
$$r = \sqrt{(x - x')^2 + (y - y')^2}$$

$$gd = \int_{\Omega'}\int_{\Omega} \ln(r)\, d\Omega\, d\Omega'$$

$$gd = \int_{y'=y_1'}^{y_2'}\int_{y=y_1}^{y_2}\int_{x'=x_1'}^{x_2'}\int_{x=x_1}^{x_2} \ln\sqrt{(x - x')^2 + (y - y')^2}\; dx\, dx'\, dy\, dy'$$

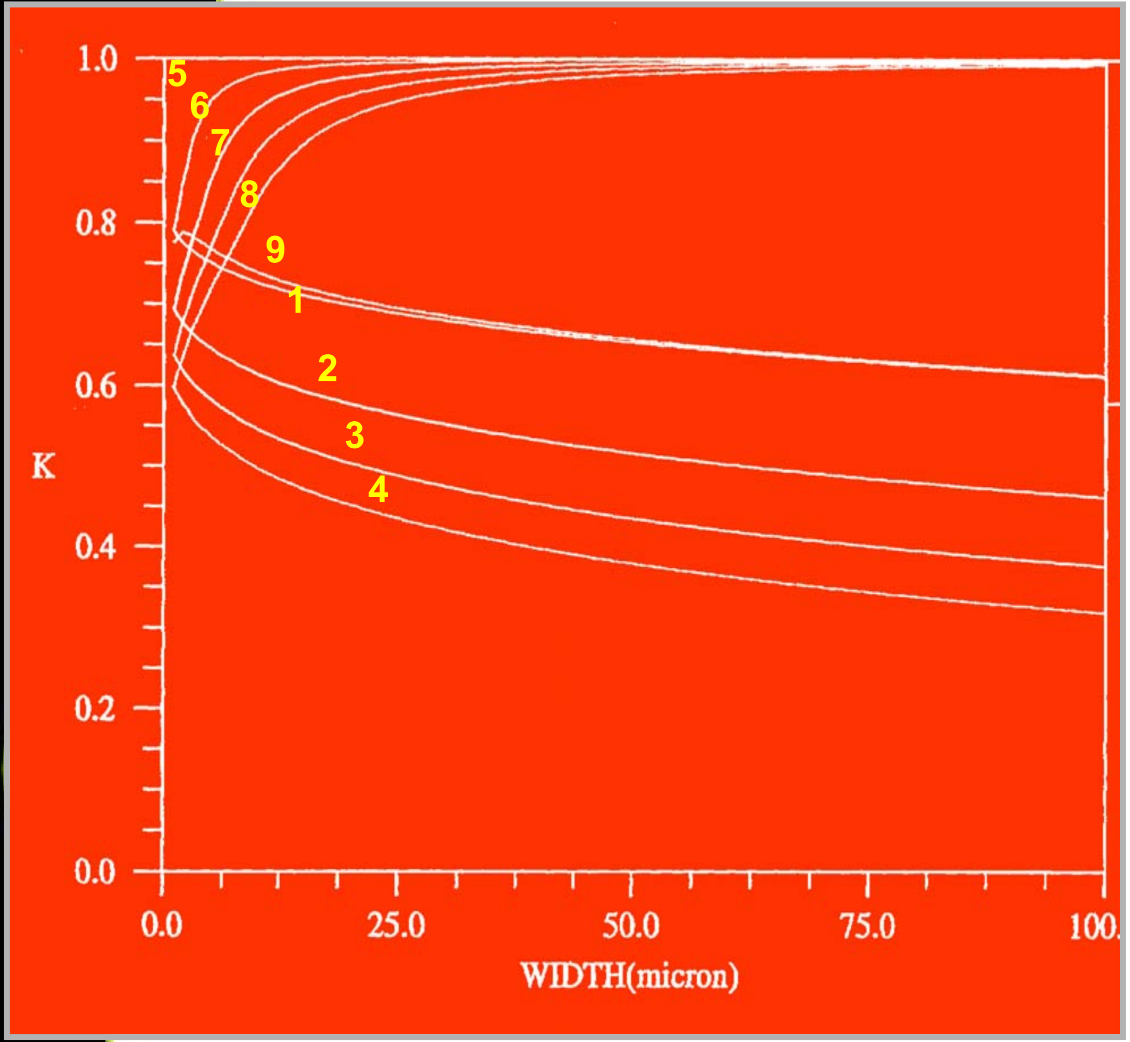
Inductive Coupling: Spirals and Helices



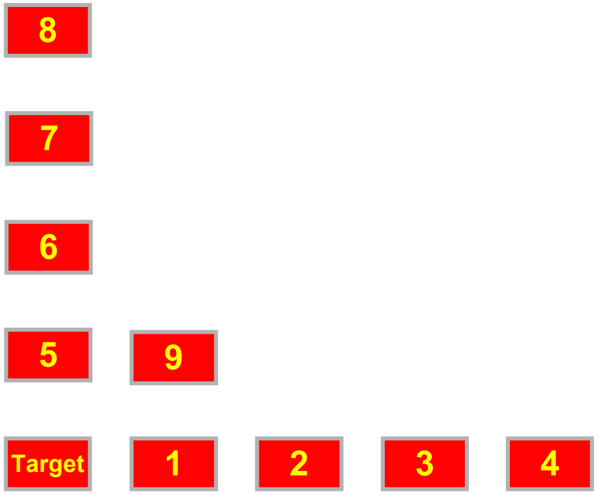


Target and Nine Conductors are all the Same Width

Mutual Inductive Coupling as a Function of Width



$$K_{nm} = \frac{L_{nm}}{\sqrt{L_{nn} \cdot L_{mm}}}$$



Detractors from Q

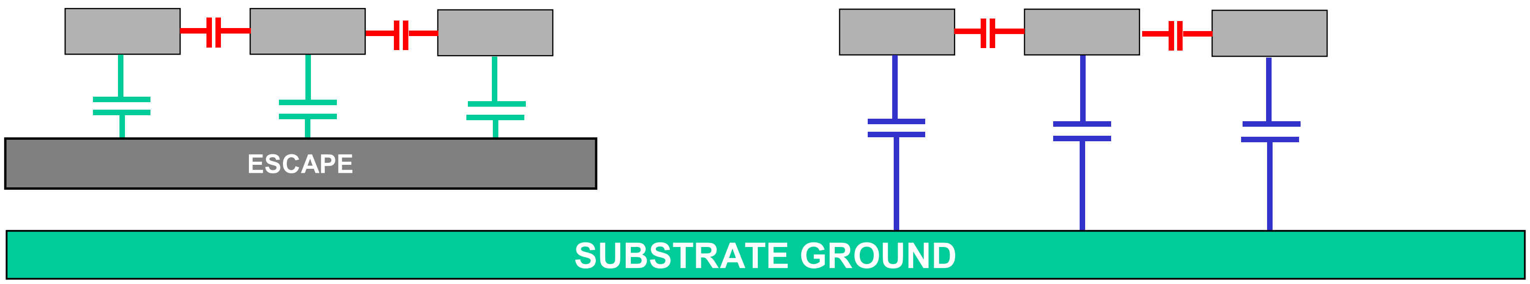
Capacitive effects

Skin and Proximity effect in Conductors

Eddy and Displacement Currents in Substrate

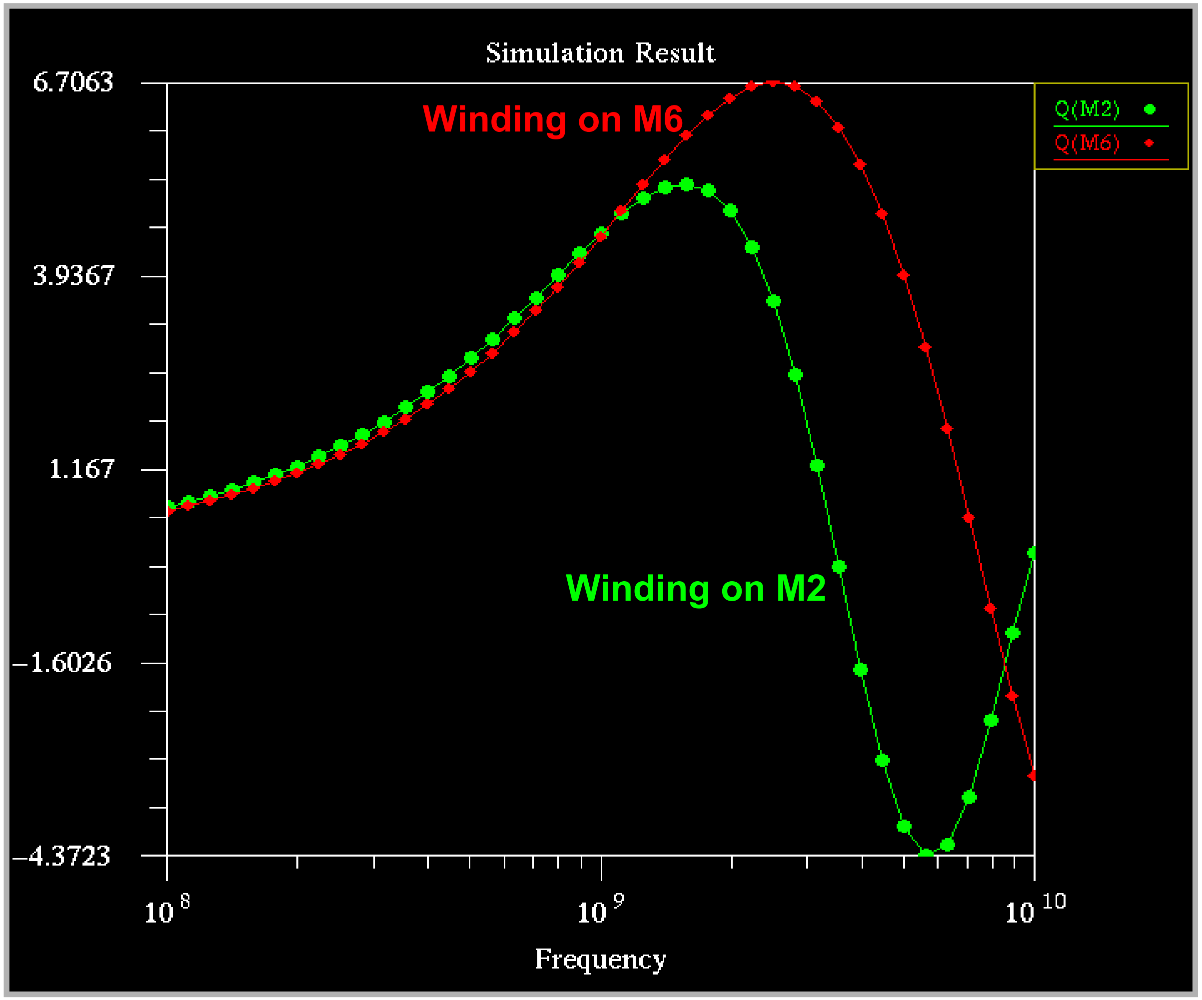
Radiative Losses

Simple Capacitance Model of an Inductor



- **Capacitance to Ground**
  - Increases with width
  - Increases with spacing
  - Use highest metal level
- **Capacitance between windings**
  - Less important for Si substrate
- **Capacitance between winding and escape**
- **Capacitance within substrate**

Q vs. Frequency for Two Inductors
(All metal layers have same thickness and ρ)

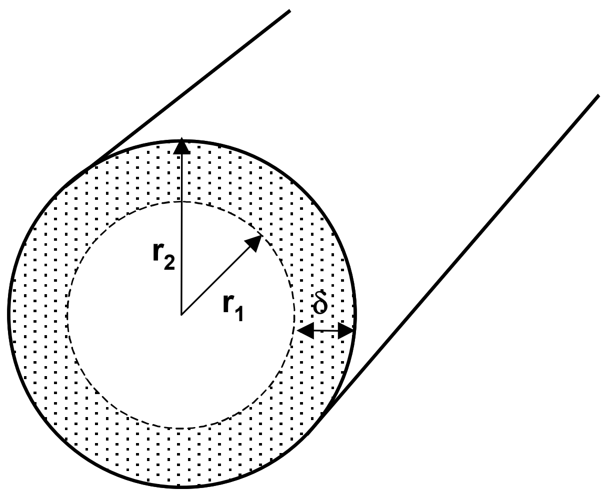


Skin Depth Area of a Conductor

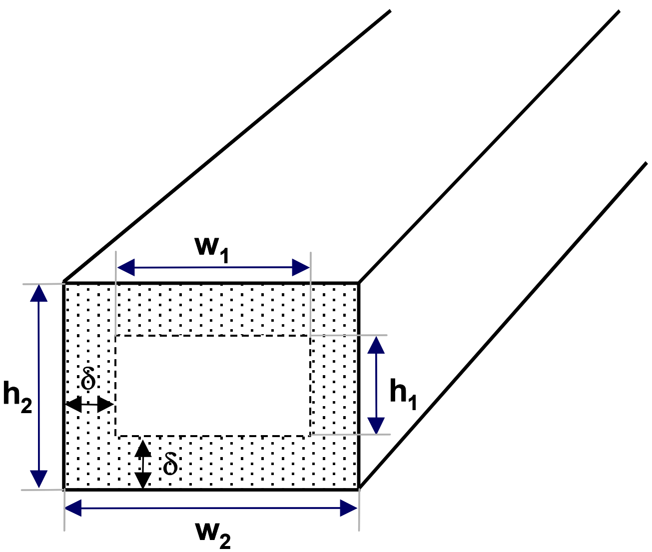
$$A_1 = \pi r_1^2$$
$$A_2 = \pi r_2^2$$
$$\text{Skin Depth Area} = A_2 - A_1 = \pi(r_2^2 - r_1^2)$$

$$A_1 = w_1 h_1$$
$$A_2 = w_2 h_2$$
$$\text{Skin Depth Area} = A_2 - A_1 = w_2 h_2 - w_1 h_1$$

$$\delta = r_2 - r_1 \qquad \delta = \sqrt{\frac{2}{\omega\mu\sigma}} \qquad 2\,\delta = w_2 - w_1 = r_2 - r_1$$

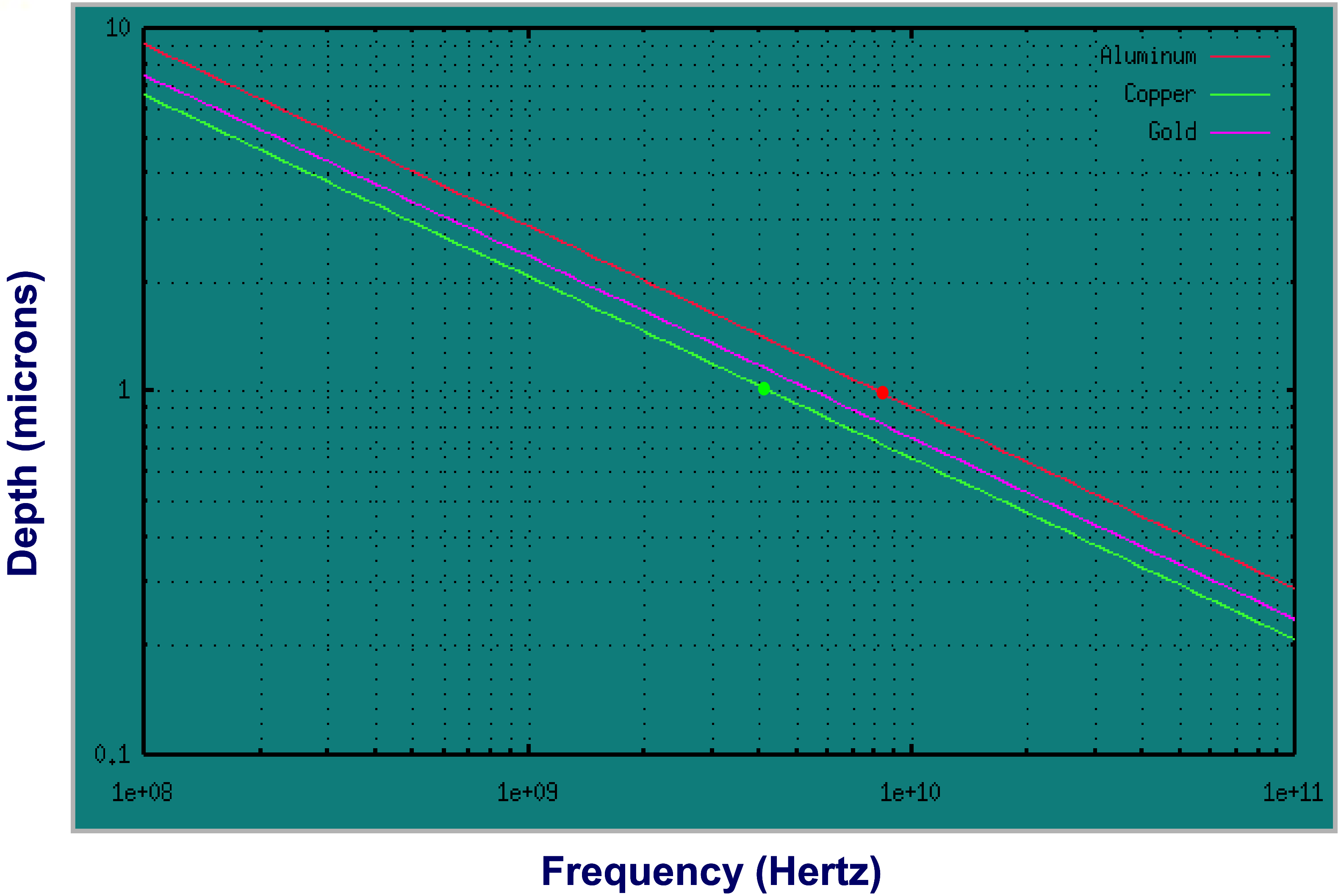


RF current flow in shaded region



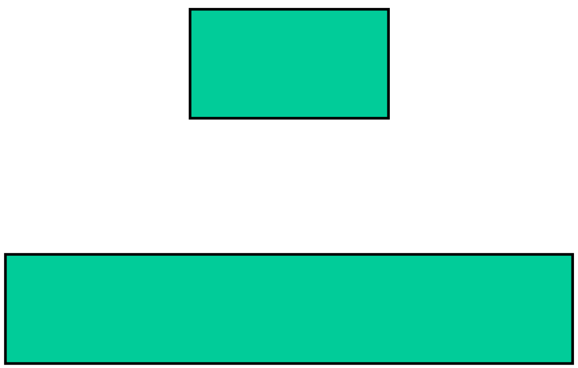
RF current flow in shaded region

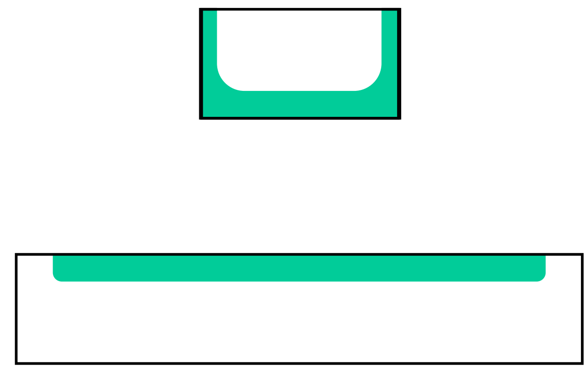
Skin Depth of Commonly Used Metals



Skin Effect in Conductors

Example shows currents in opposing directions.



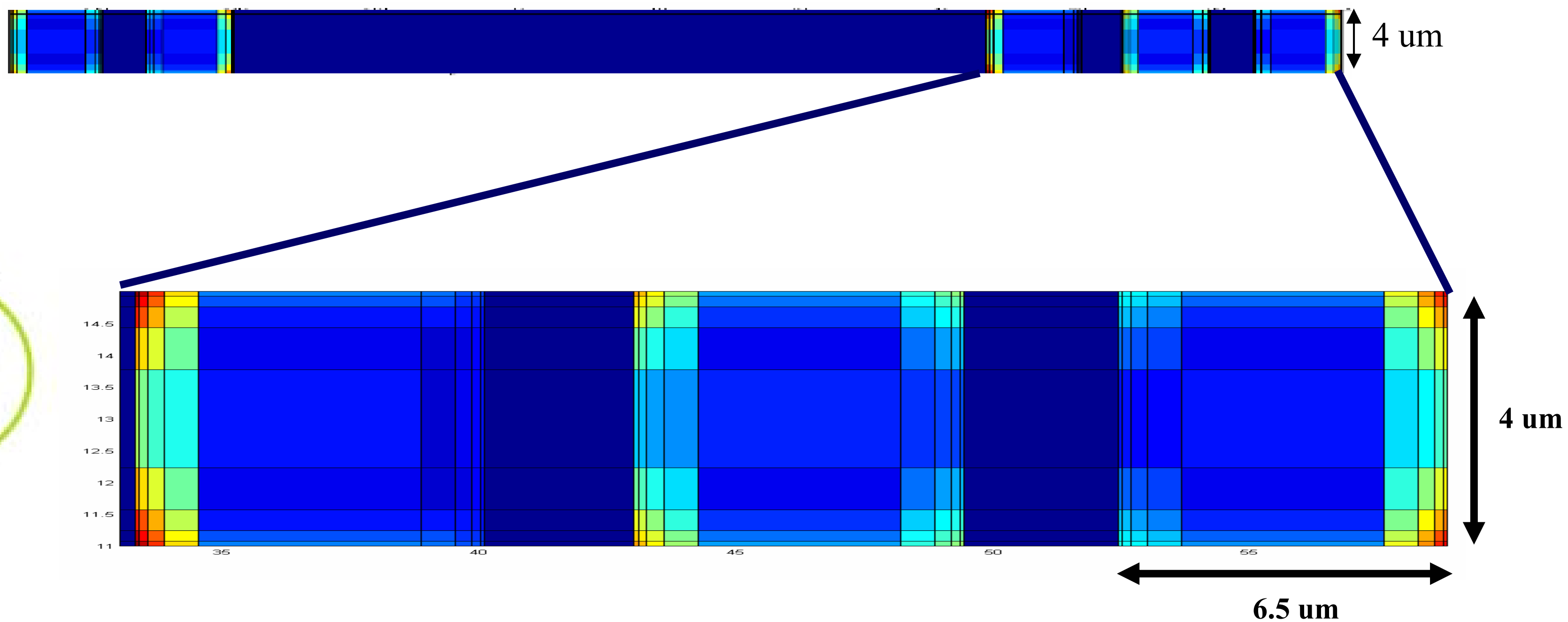


Low frequency currents are distributed across the entire cross sectional area to take path of minimum resistance.

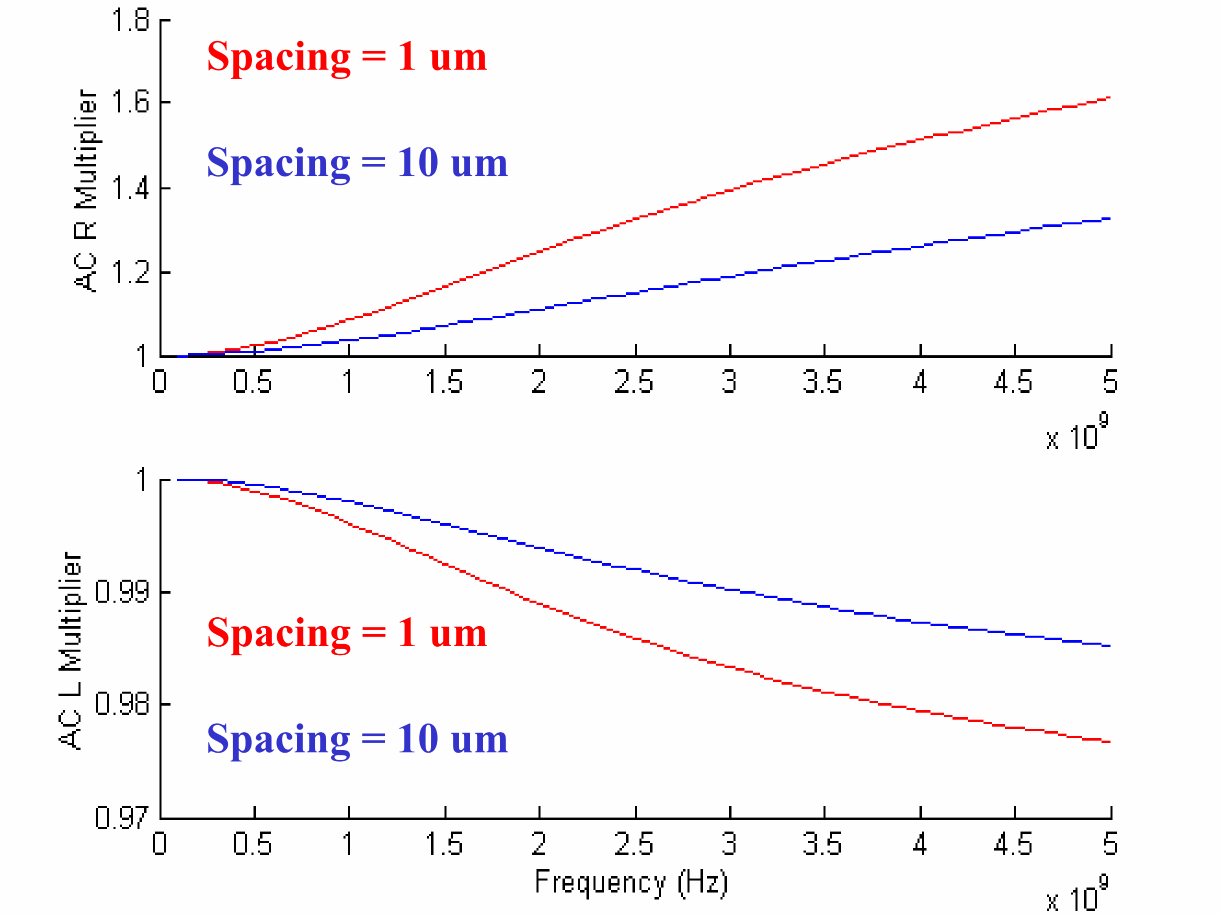
High frequency currents are distributed to minimize mutual inductance thus minimizing impedance.

Current Distribution
Due to Skin and Proximity Effects

2.5 Turn Square Spiral
100 um Inner Diameter
6.5 um Width
4 um Thickness
2.1 um Spacing

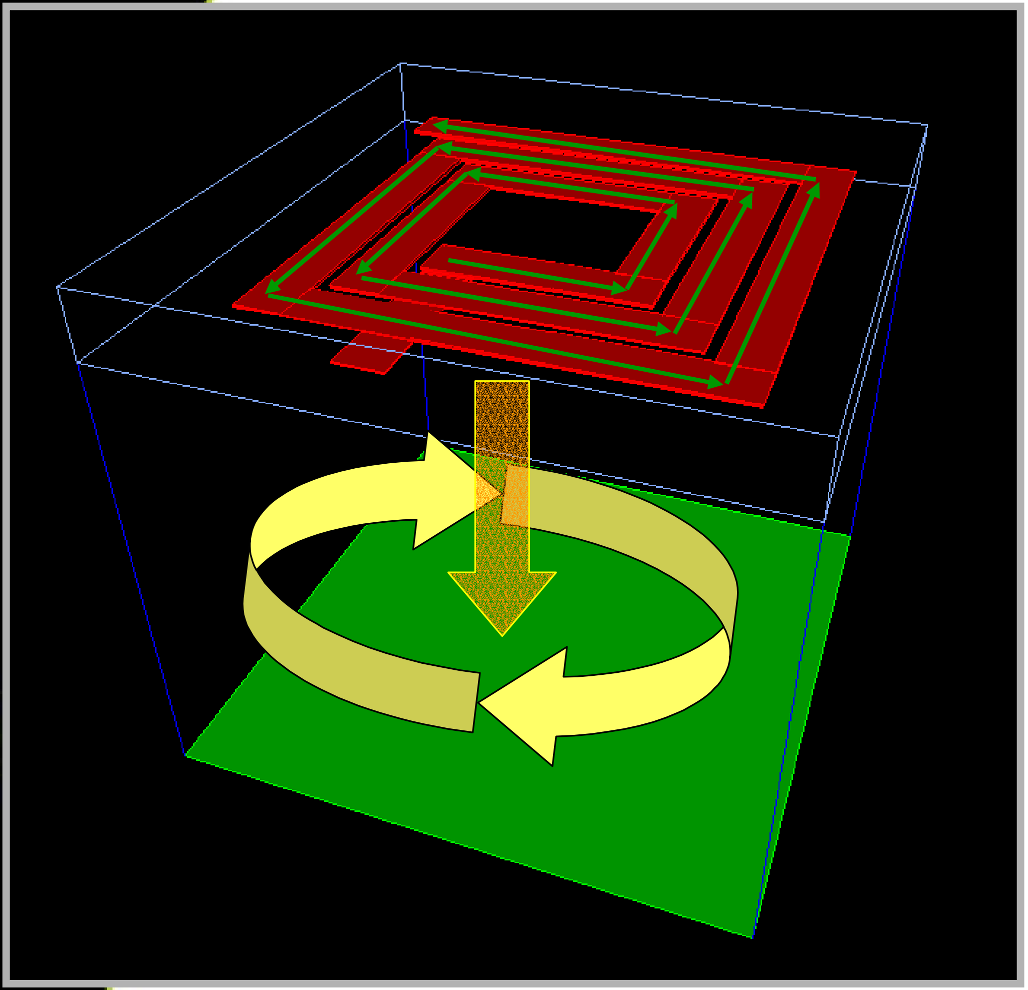


AC Resistance & Inductance Comparison For 1um and 10um Spacing



Five Turns, Outer spiral diameter = 200 um, Width = 10 um

Reducing Substrate Losses
(Some Partially Useful Methods)



- Use high resistivity substrate
- Patterned shields
  - Limited Use
  - Significant Noise coupling
  - Reduced operating frequency
- Depletion region
- Keep inductor small

Radiative Losses

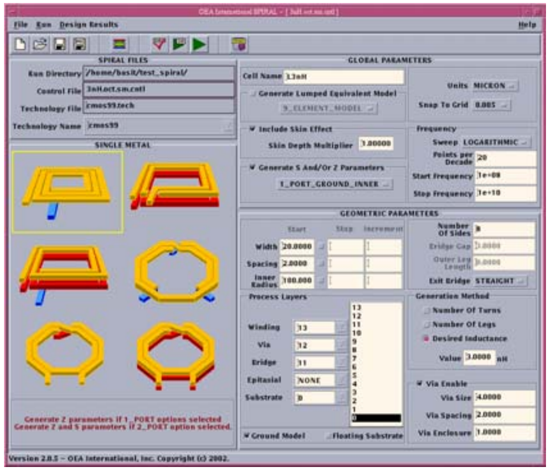
- On chip inductors make very poor antennas
  - No need to worry about radiation loss in most cases
  - However, should be careful near quarter wavelength

V_p = Propagation Velocity = Phase Velocity

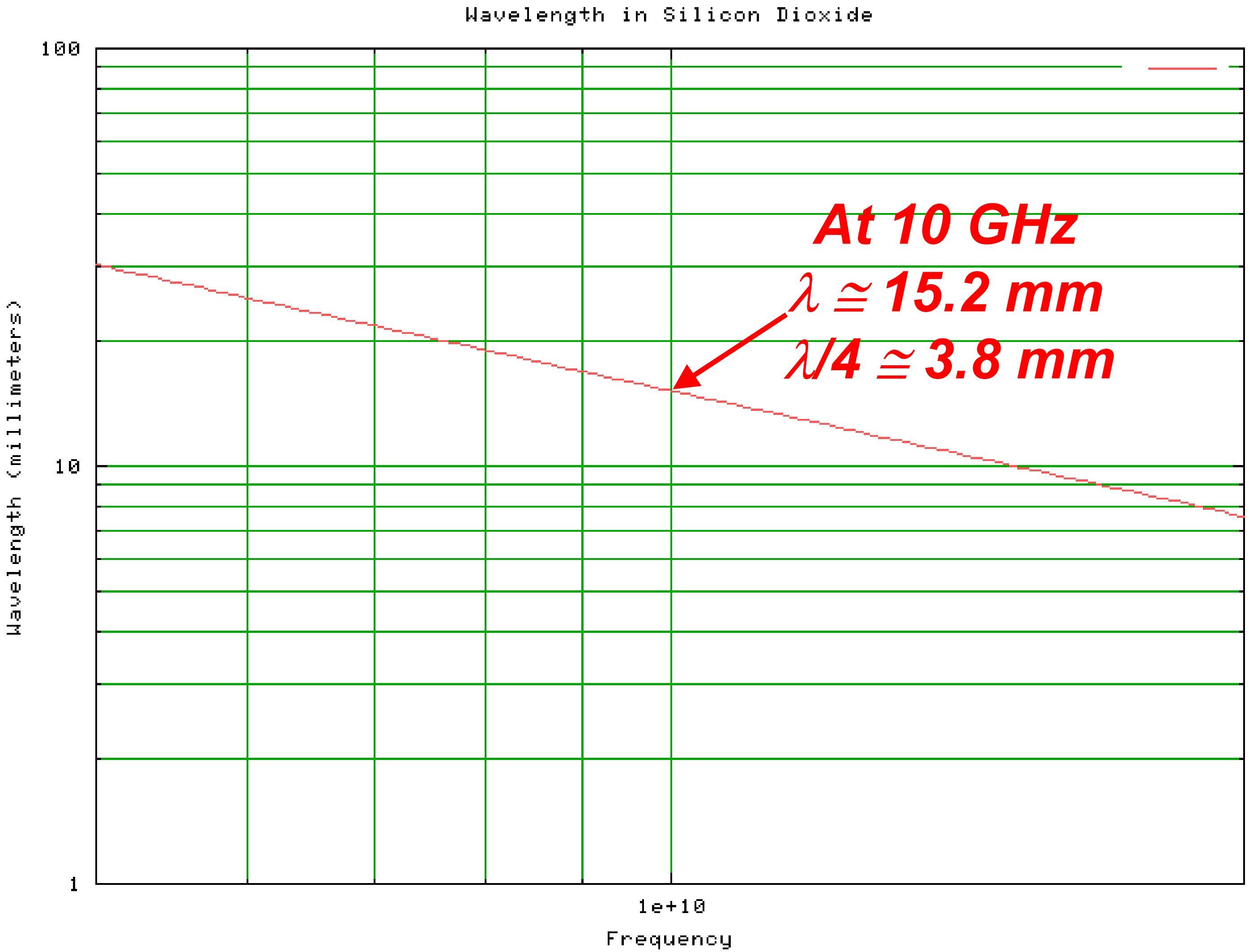
$$V_p = 1/\sqrt{\mu\varepsilon} = 1/\sqrt{LC}$$

$$V_p = f\lambda$$

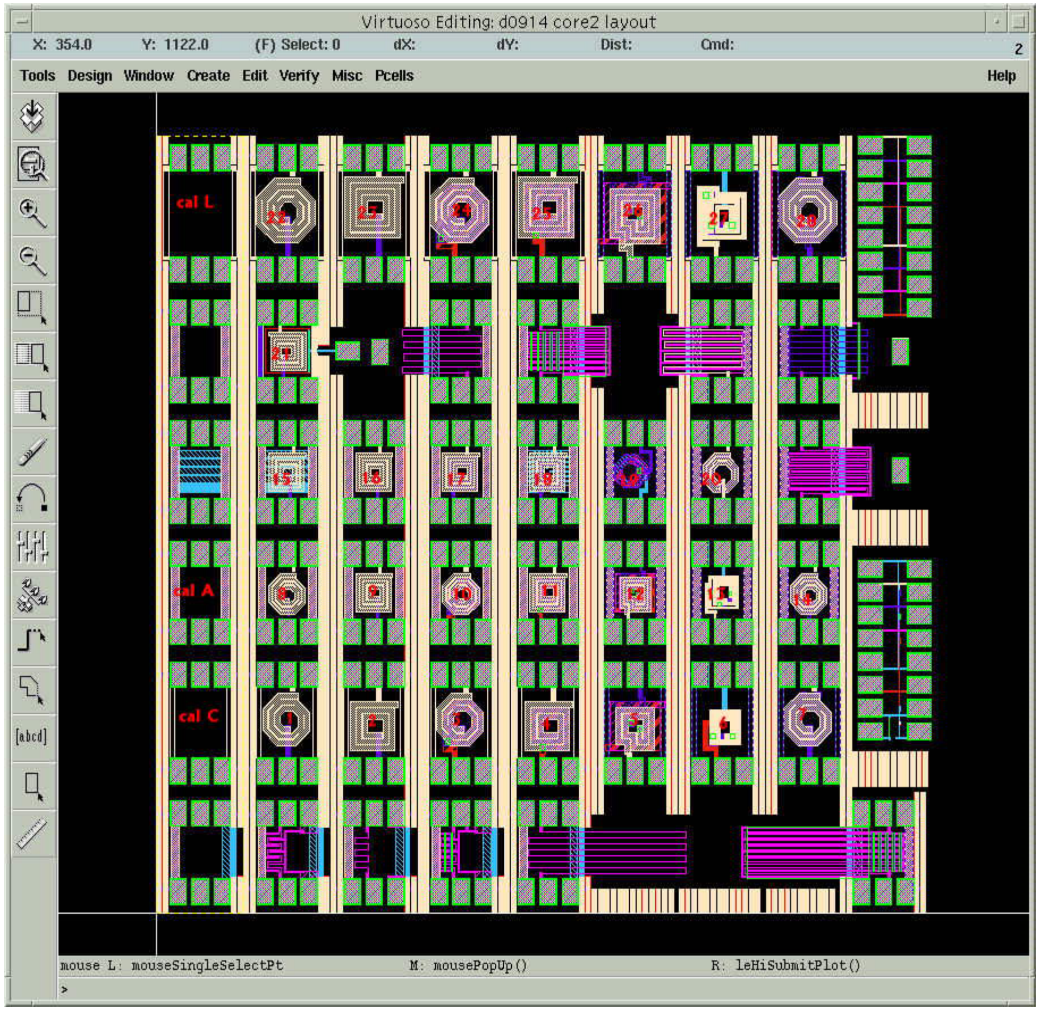
$$\lambda = (1/\sqrt{\mu\varepsilon}) / f$$

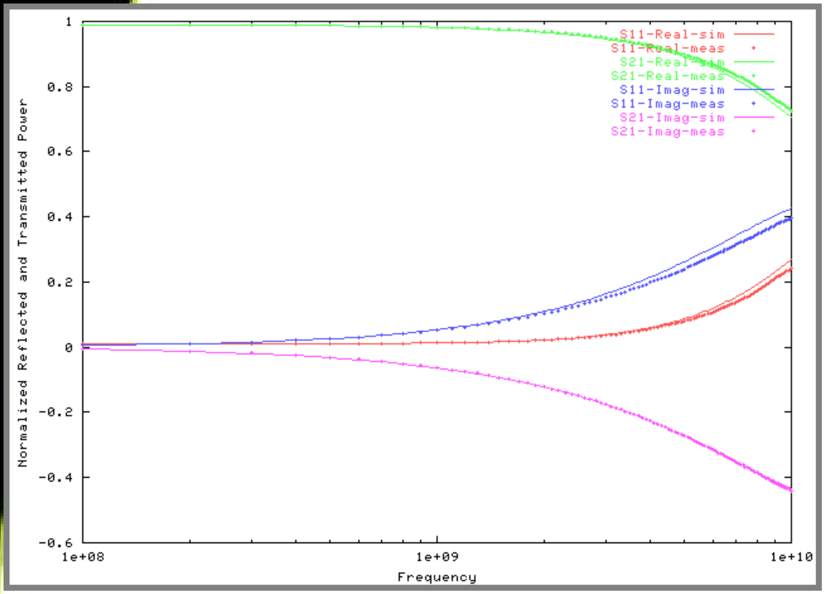


Wavelength vs. Frequency in SiO_2

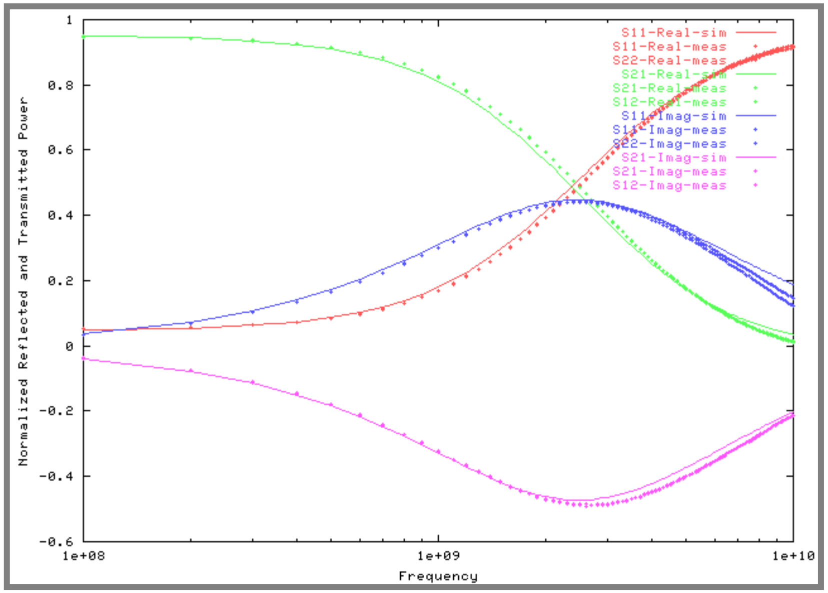


Validate Using Test Chips





Measured vs Simulated ~ 1 nH



Measured vs Simulated ~ 7 nH

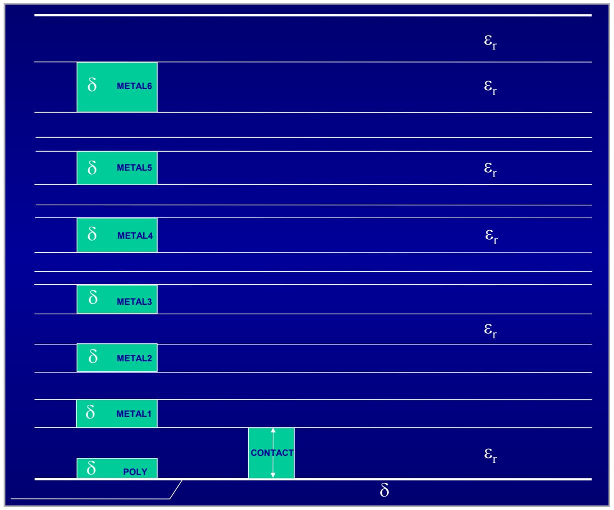
A Real Design

Start with what Designer knows:

- Physical Process Description
- Frequency Range or desired frequency
- Desired Inductance
- Minimum Acceptable Quality Factor

Process Technology File

```
// spiral technology file:
//*******************************************************************
technology CMOS
units microns
metal
layer     0   -300.0       -1.0e+00      0.1        //gnd
layer     5   -1.0          0            10         //epi
layer     8    1.2          1.7          3.3e-6     //met1
layer     9    1.7          2.3          6.0e-05    //via1
layer    10    2.3          2.8          3.3e-6     //met2
layer    11    2.8          3.4          6.0e-05    //via2
layer    12    3.4          3.9          3.3e-6     //met3
layer    18    3.9          4.5          6.0e-05    //via3
layer    19    4.5          5.0          3.3e-6     //met4
layer    20    5.0          5.6          6.0e-05    //via4
layer    21    5.6          6.5          3.3e-6     //met5
layer    22    6.5          7.1          6.0e-05    //via5
layer    23    7.1          9.2          3.3e-6     //met6
endmetal
dielectric
layer     1    0.000        10.0         3.9     //oxide
layer     2   10.000        11.0         6.0     //nitride
enddielectric
endtechnology
```



A Real Inductor Design

Example Design Specification:

- Frequency Range -- Example 2 GHz through 3 GHz
- Desired Inductance -- 3 nH
- Need Quality Factor > 8 @ 2.4 GHz

- Impedance at 2.4GHz = 2*pi*F*L = 45 Ohms

An Aside: Three Definitions of Q

- Simplest Definition: (Zero at Resonance)

$$\frac{-\mathrm{Imag}(Y_{11})}{\mathrm{Real}(Y_{11})}$$

- 3-dB Bandwidth Definition:

$$\frac{\omega_o}{2}\frac{d\phi}{d\omega}\bigg|_{\omega_o}$$

- Most General Definition

$$\frac{\text{Energy Stored}}{\text{Energy Dissipated}}\bigg|_{\text{one cycle}}$$

A Real Design: Starting Questions

- What topology to use?
  - Helix, spiral, symmetric, number of sides
- Which metal(s) to use for winding and bridge?
  - Single metal, double metal, series or parallel metals
- What length, width and inner radius to use?

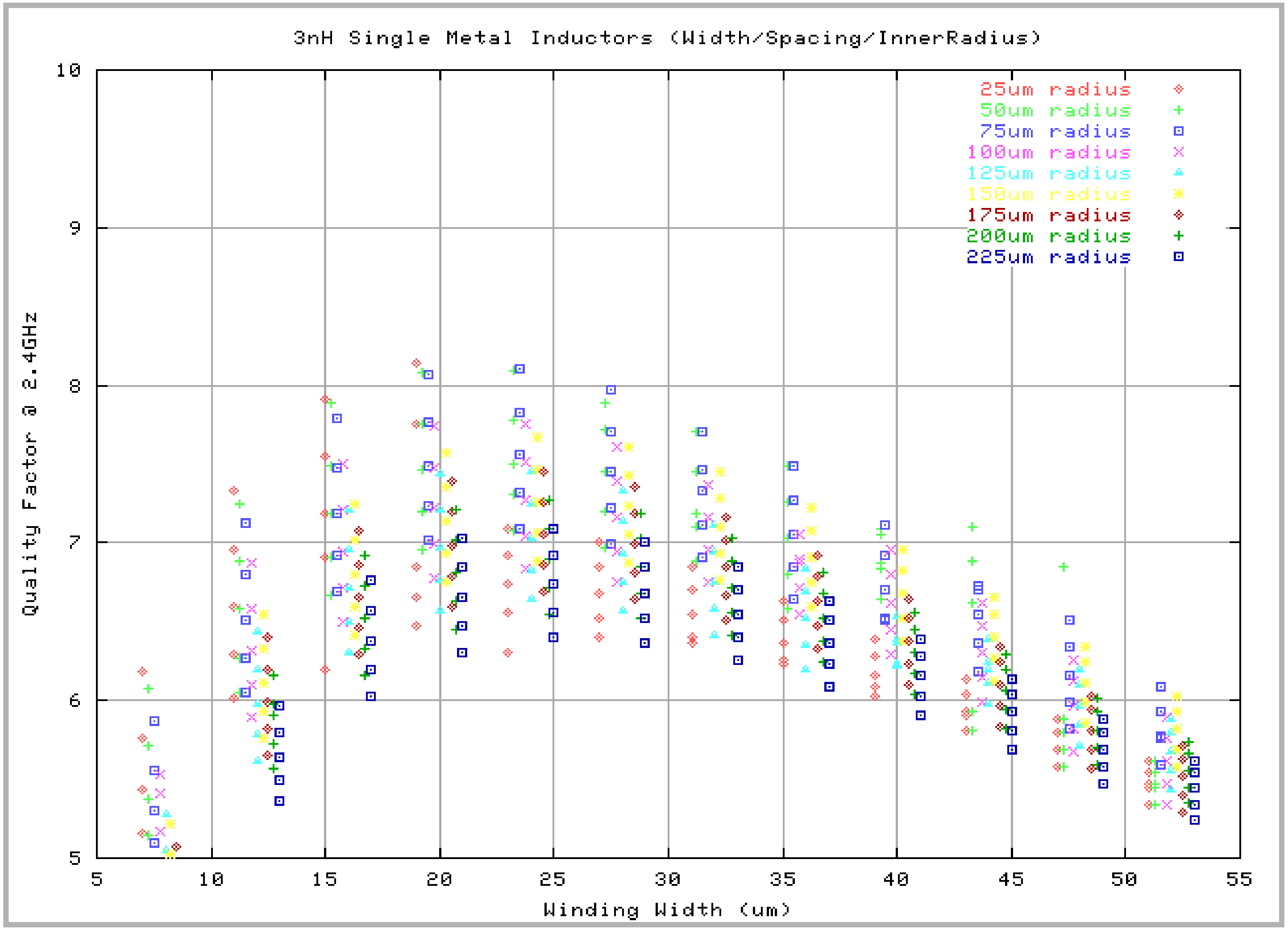
SPIRAL Control File

```
CELL L3nH
TARGET ind
*GROUND_LAYER 0 5
GROUND_LAYER 0
PLANAR
UNITS MICRON
SOLVE
GROUND_TYPE TARGET_ONLY
*FLOAT
SKIN
1PORT
FREQUENCY LIN 2 2.4e+9
   2.5e+9
SNAP_TO_GRID 0.05
```

```
SPIRAL ind
ESCAPE STRAIGHT
TYPE DOUBLE_METAL
SIDE_NUMBER 8
CHOICE L
DESIRED_INDUCTANCE 3.0e-09
WIDTH                :-<) 8 52 4 (>-:
SPACING              :-<) 2 10 2 (>-:
INNER_RADIUS       :-<)25 225 25 (>-:
BRIDGE_GAP 3
SPIRAL_LAYER 23
VIA_LAYER 22
BRIDGE_LAYER 21
ORIGIN 0.0 0.0
*VIA_SIZE 2
*VIA_SPACING 2
*VIA_ENCLOSURE 1
ENDSPIRAL
```

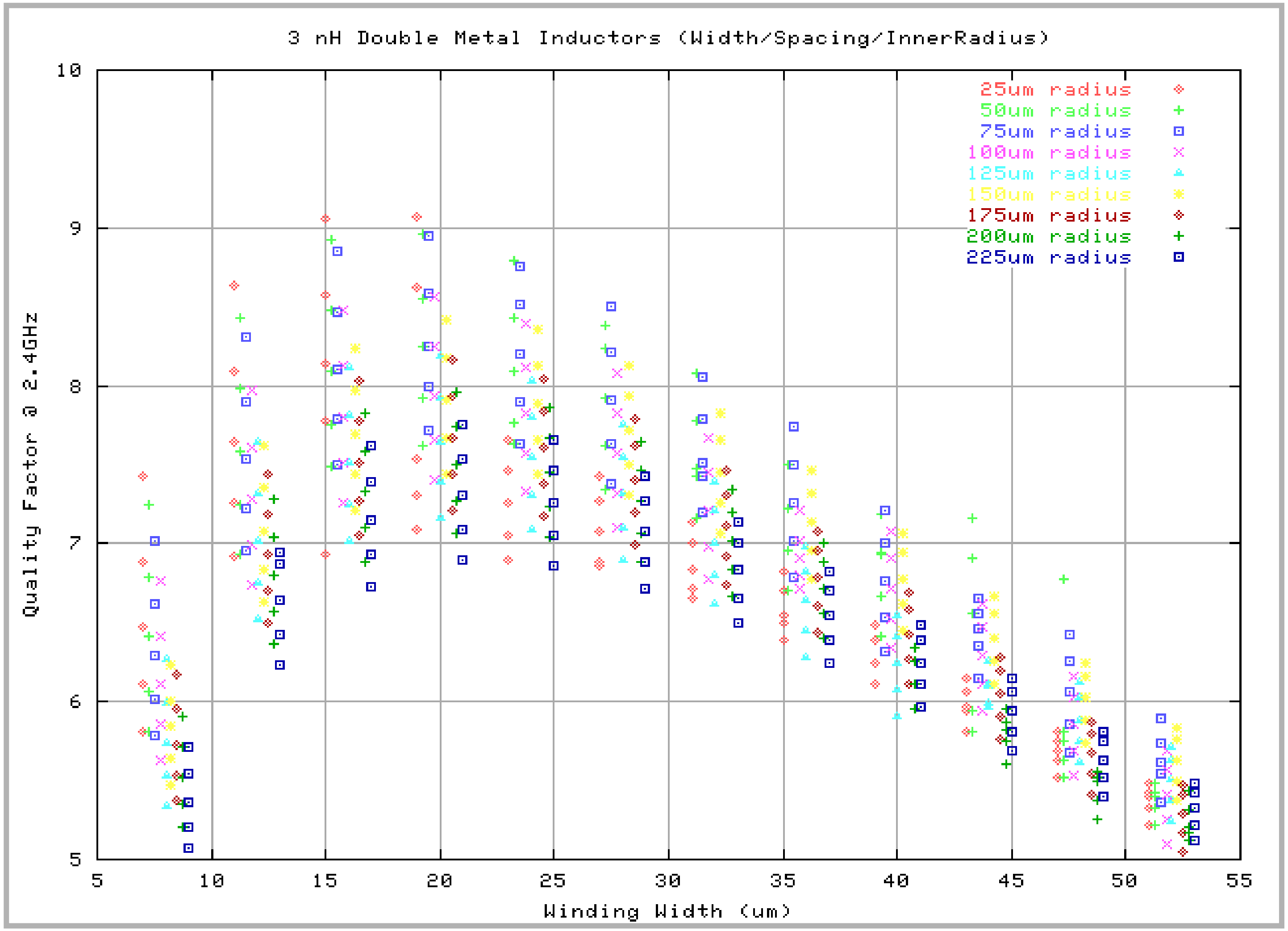
SPIRAL Output 3nH

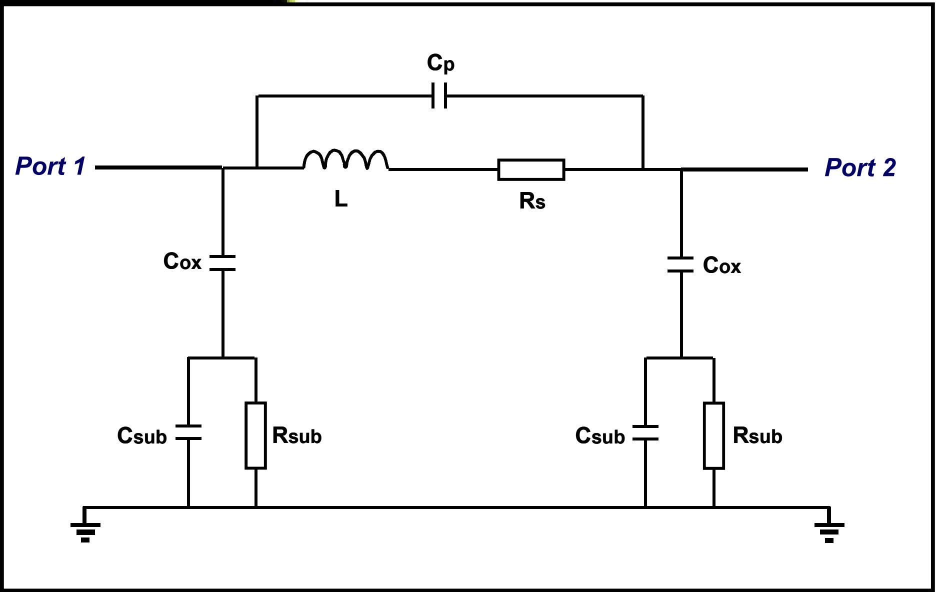
Single Metal - Octagon



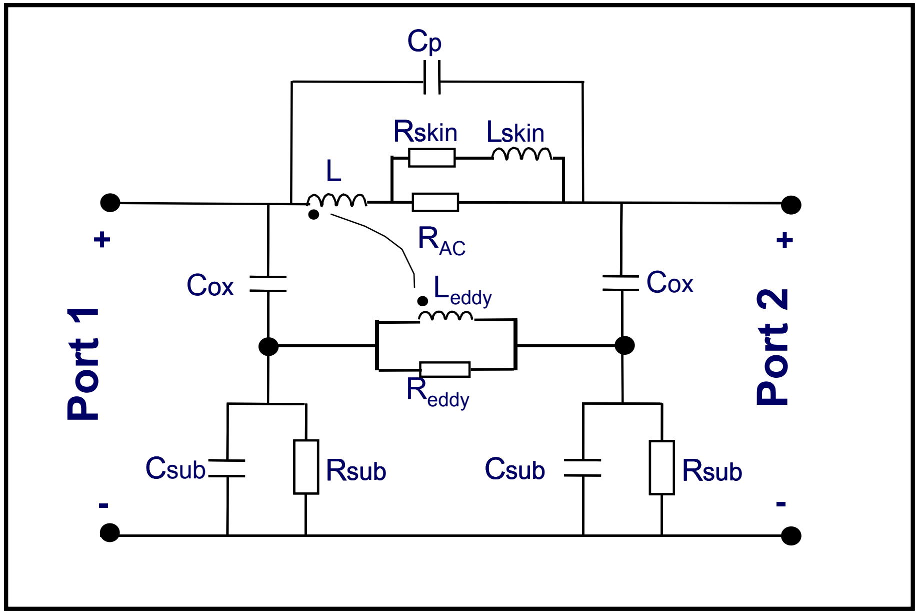
SPIRAL Output 3nH

Double Metal - Octagon



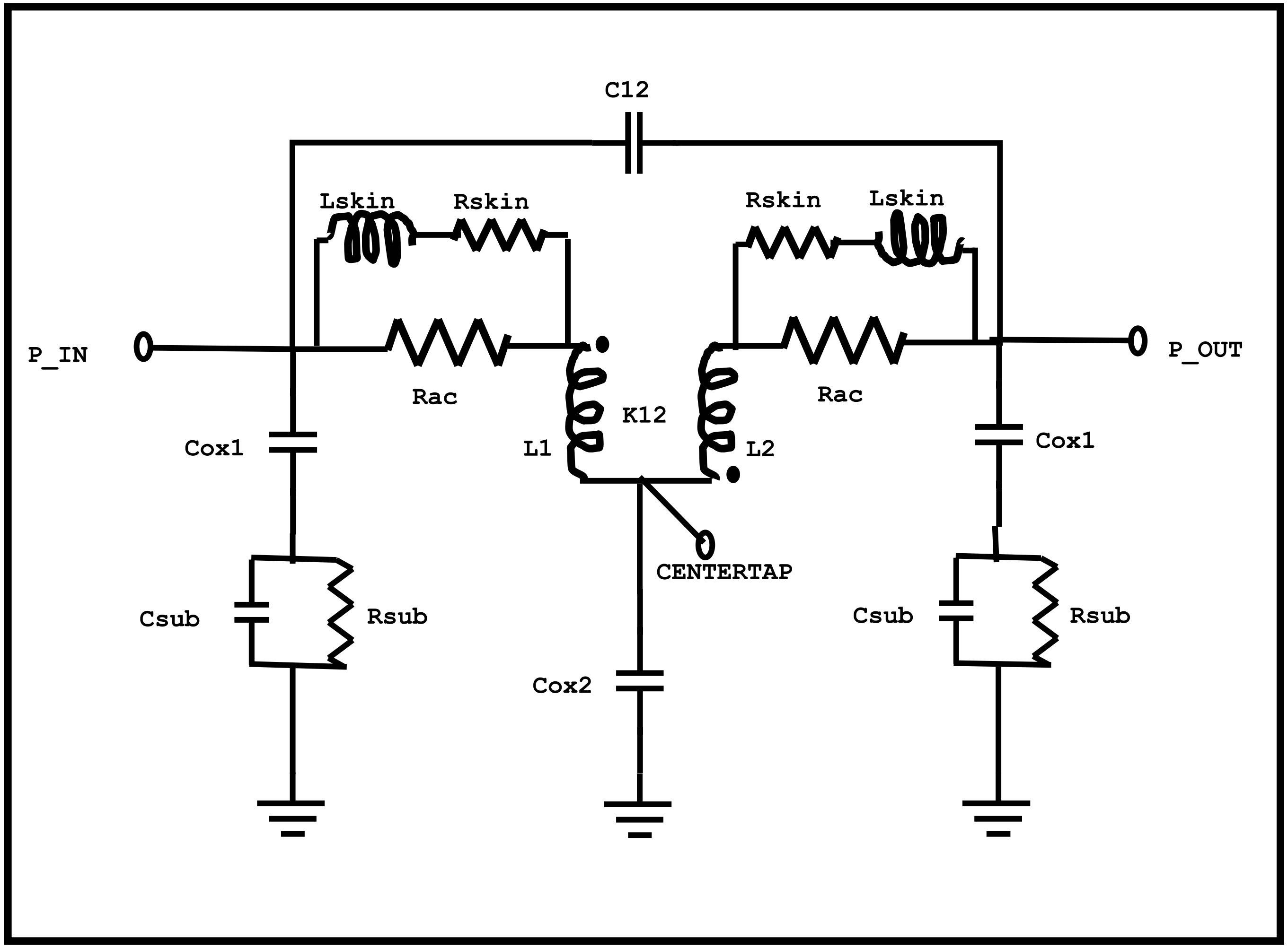


Model Fitting:
Simple 9 Element Model



Enhanced 13 Element Model
Plus 1 Inductive Coupling

Symmetric Inductor
Lumped Model

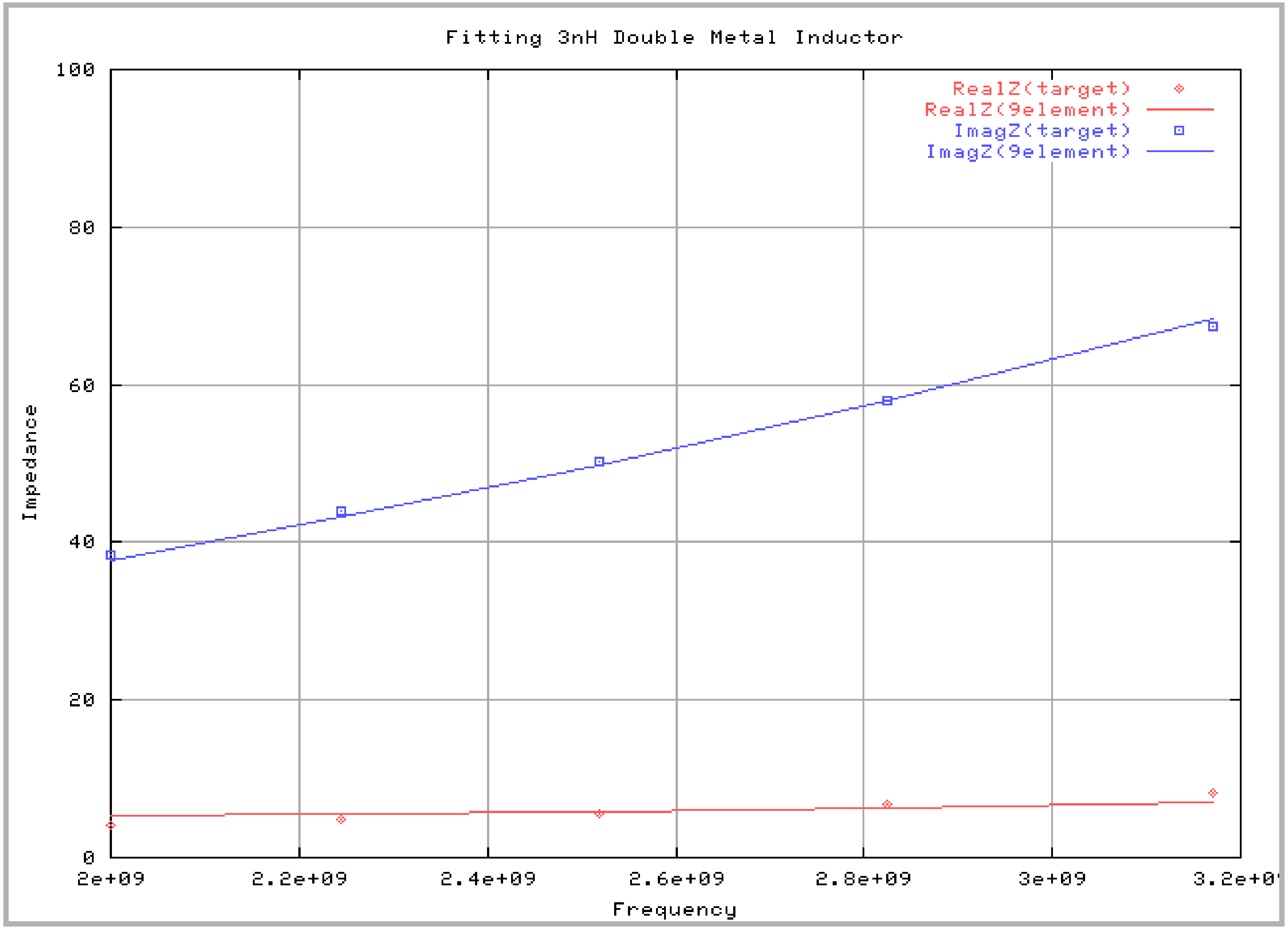


SPIRAL Control File: Fitting

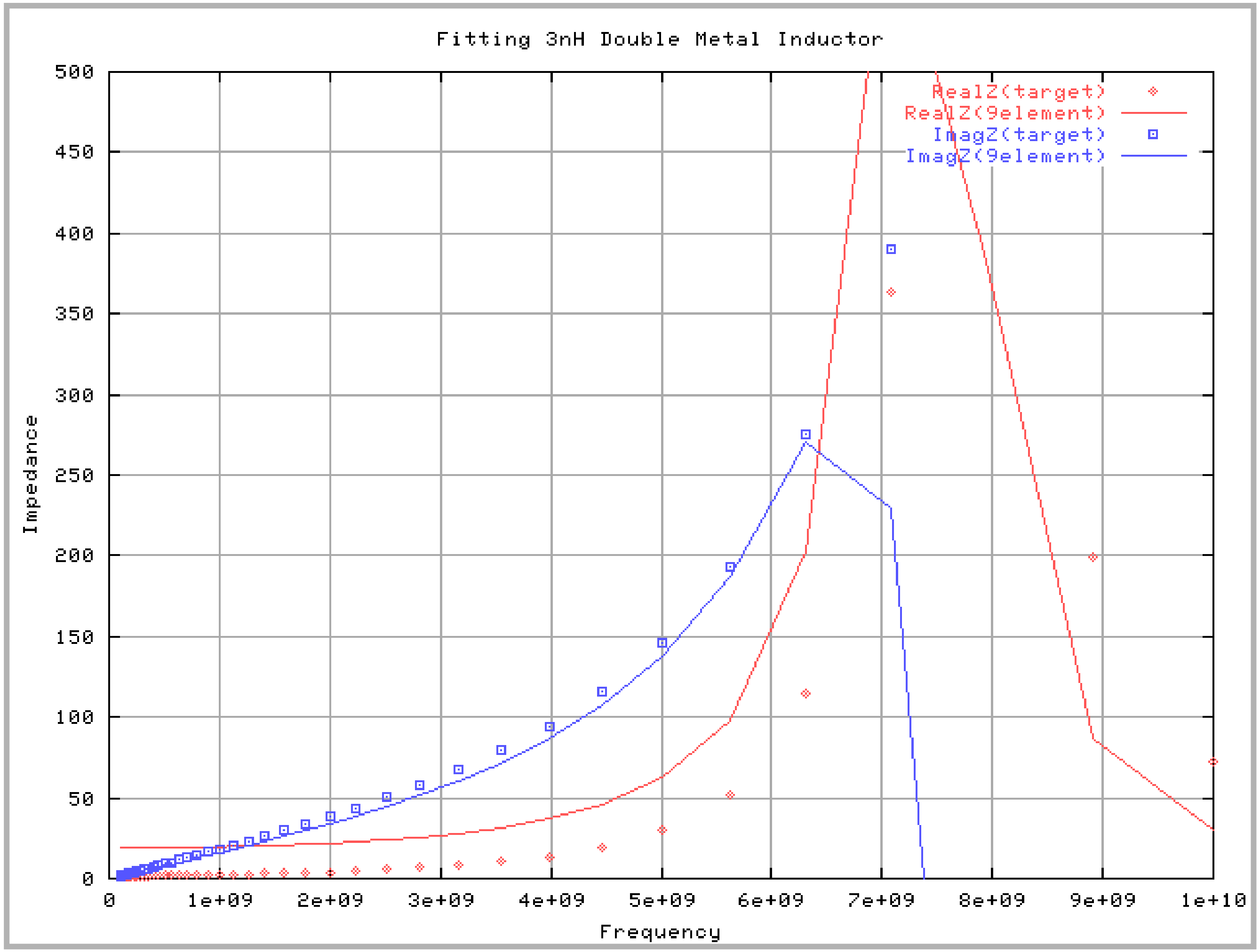
```
CELL L3nH
TARGET ind
*GROUND_LAYER 0 5
GROUND_LAYER 0
PLANAR
UNITS MICRON
SOLVE
GROUND_TYPE TARGET_ONLY
*FLOAT
SKIN
1PORT
FREQUENCY DEC 20 1e+8 10e+9
*FREQUENCY DEC 20 2e+9 3e+9
SNAP_TO_GRID 0.05
FIT_MODEL9
*FIT_MODEL13
*FIT_SYMMETRIC
```

```
SPIRAL ind
ESCAPE STRAIGHT
TYPE DOUBLE_METAL
SIDE_NUMBER 8
CHOICE L
DESIRED_INDUCTANCE 3.0e-09
WIDTH 20
SPACING 2
INNER_RADIUS 25
BRIDGE_GAP 3
SPIRAL_LAYER 23
VIA_LAYER 22
BRIDGE_LAYER 21
ORIGIN 0.0 0.0
VIA_SIZE 2
VIA_SPACING 2
VIA_ENCLOSURE 1
ENDSPIRAL
```

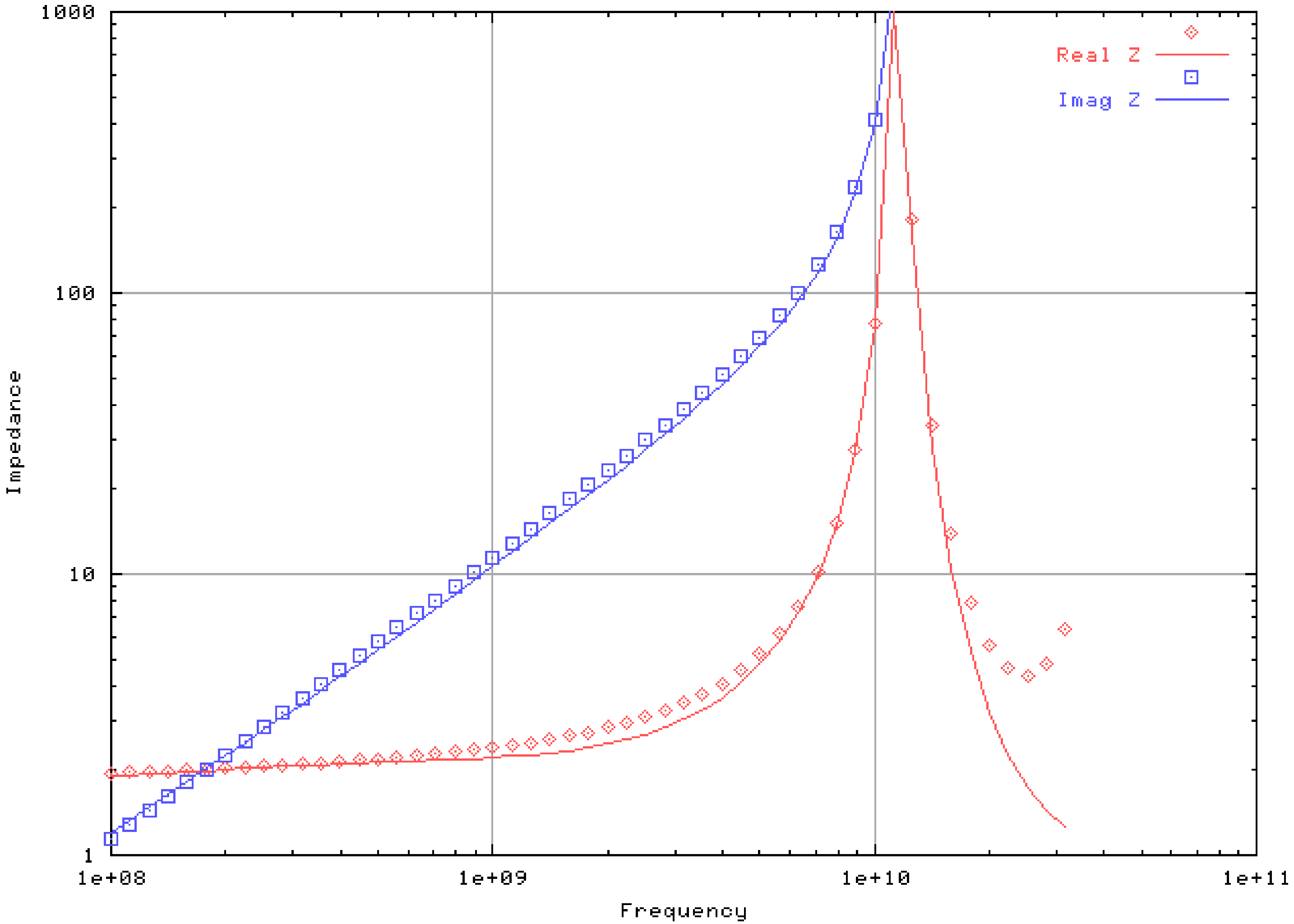
Narrow Band 9 Element Model Fit



Broadband 9 Element Model Fit



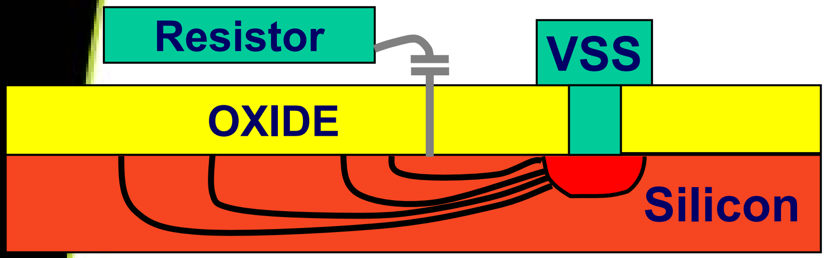
Broadband 13 Element Model Fit

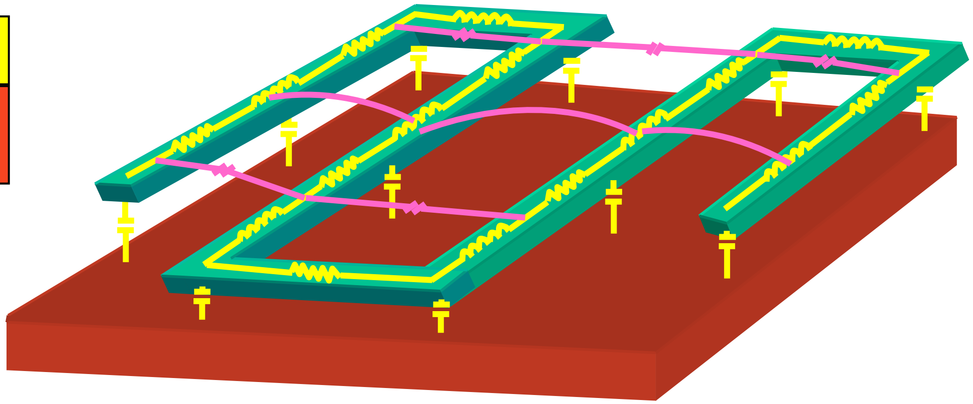


Resistive Components

Thin Film Resistors (Not as Simple as they Look)

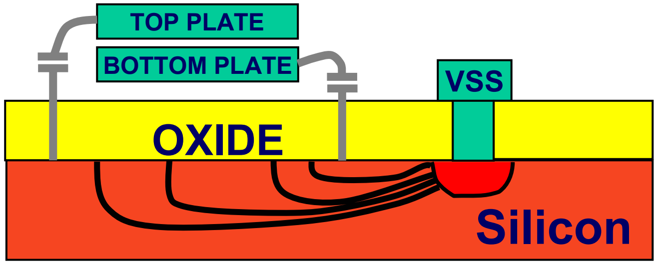
- Large Devices with Distributed Resistance and Capacitance
- Could Include Significant Substrate Effects
- Asymmetry Could Cause Noise Pickup from Substrate



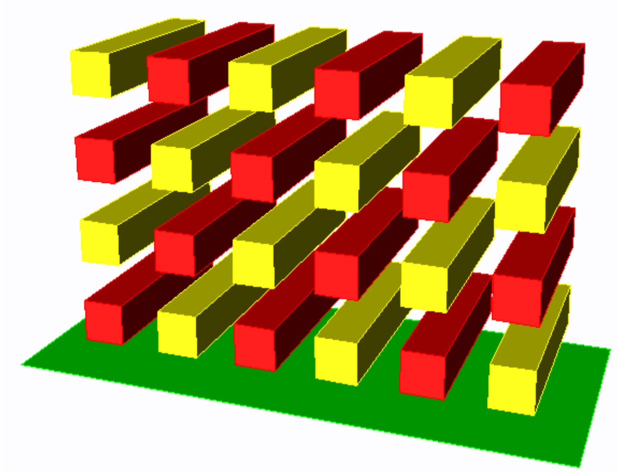


- **What is the coupling across segments?**
- **What is the coupling through the substrate?**

Capacitive Components

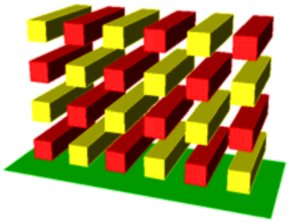


- **MIM Capacitors**
  - Large distributed structures
  - Asymmetric with respect to substrate
- **Multi-layer Interdigitated Capacitors**
  - OEA Patented technique
  - Optimize Q, Capacitance Density, Parasitic Capacitance, etc…
  - Symmetric relative to substrate (minimize noise pickup from substrate)
  - Include skin and proximity effects
- **Control of undesired effects**
  - Minimize non-linear behavior
  - Eliminate high resistance well contact
  - Optimize selection and usage of metals
  - Optimize finger width and spacing
  - Optimize placement of metal straps

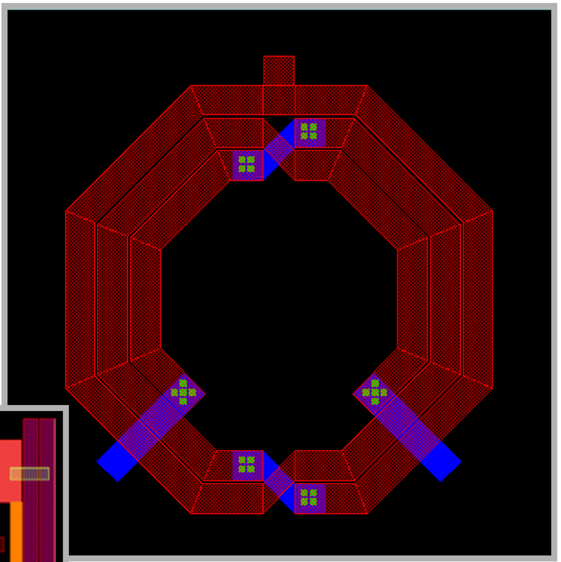


Multi-layer Interdigitated Capacitors

Finger W/S(μ)	Finger L (μ)	Capacitance (fF)	Density (fF/μ^2)	Parasitic Cap (%)
0.080	5.2	300	9.70	1%
0.100	6.5	321	6.64	1%
0.120	7.8	326	4.69	1%
0.150	9.8	340	3.13	2%
0.200	13.0	362	1.87	3%
0.250	16.3	383	1.27	4%
0.300	19.5	411	0.95	5%
0.400	26.0	473	0.61	8%
0.800	52.0	857	0.28	14%

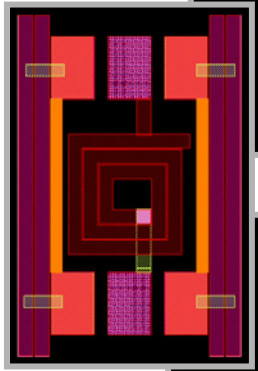


OEA RF/Analog Software Products



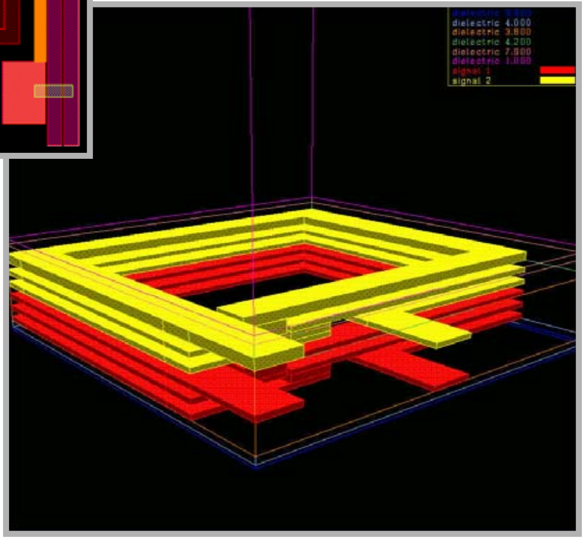
SPIRAL™

- Includes all relevant effects (skin, substrate, etc…)
- Synthesizes a large variety of inductors
- Can examine thousands of designs in a few hours
- Generates layout, Spice, Z & S parameters
- Can fit to many simplified models
- Optimization engine included



RF-PASS™

- Outputs N-Port Y, Z and S parameters
- Handles much more complex substrates and designs
- Optimization of arbitrarily complex passive structures



SUBSTRATE NOISE ANALYSIS

- Calculates full-chip substrate noise couplings
- Enables what-if exploration of isolation strategies
- Allows design planning before layout

Conclusions

- Spiral Inductor Design is Not Simple as It Looks
- Selecting a Spiral from a Pre-characterized Library Does Not Do the Job!
- It is Possible to Design a Spiral or Group of Spiral Inductors Easily with the Right Software
- High Q and Very High Capacitance Design Structures can be Designed to Save Valuable Chip Real-estate by Using the Proper Tools